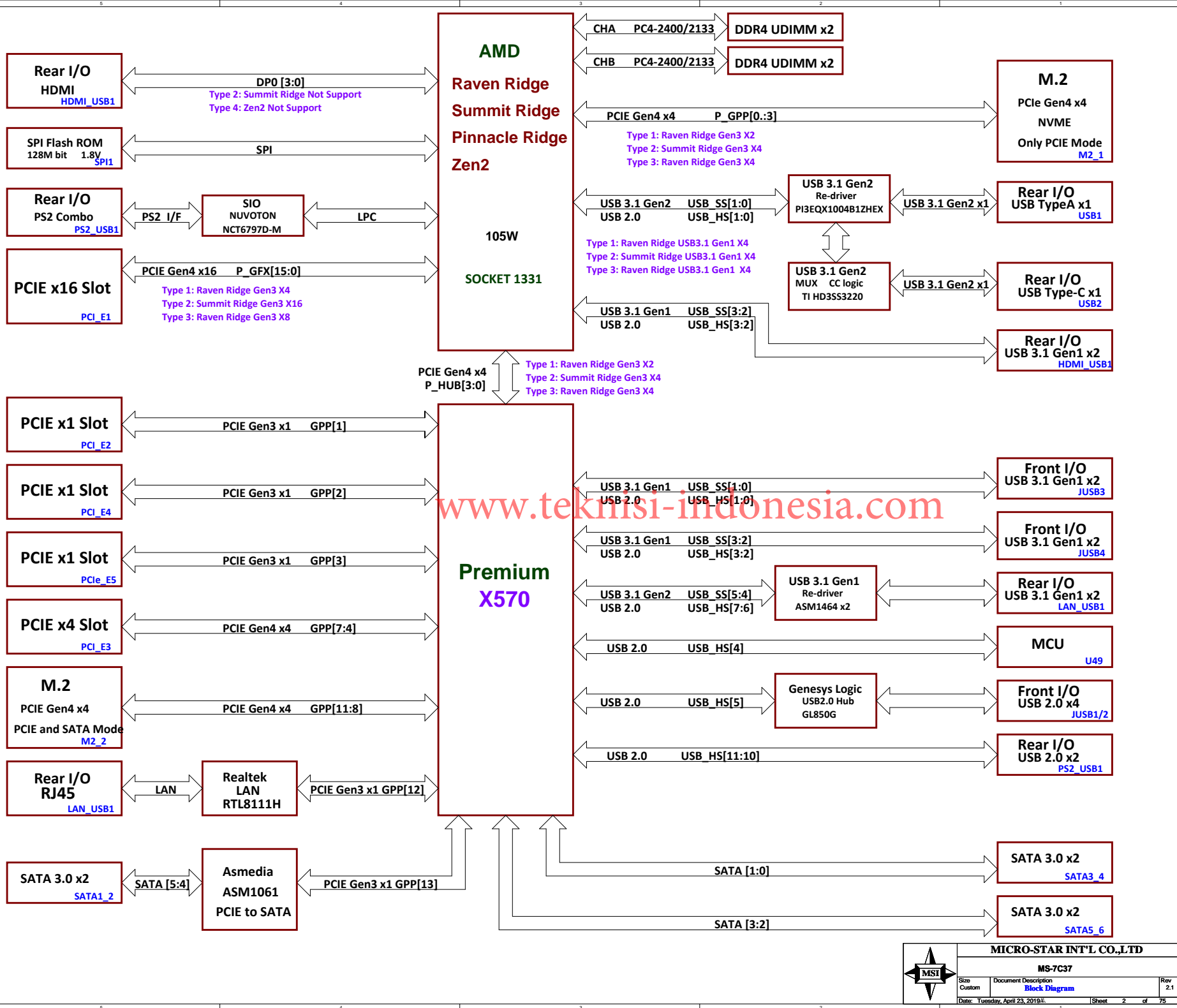
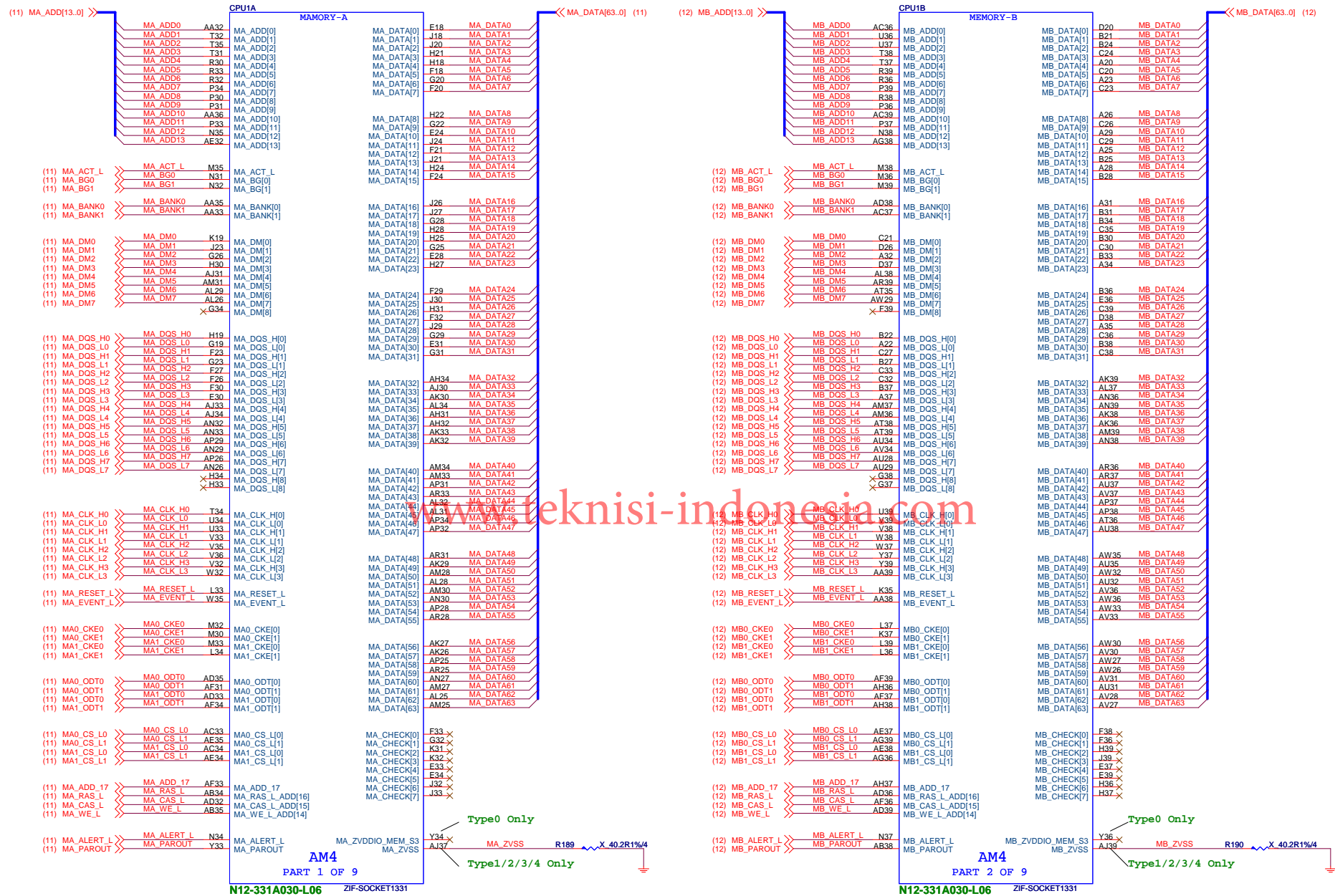


# AMD AM4

## GAMING EDGE AC

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04	AM4 PCIE / SATAE	39	USB Power - UP7501	69	LED - Mystic Light - 1
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29	SIO NCT6797D-M	59	PROM - GS7133 / 2.5V		
30	SIO HW Monitor / NCT7718W	60	OV Control - NCT3933		
31	FAN TYPE-J CPUFAN1	61	OV 12VIN - RT9553B		
32	FAN TYPE-J PUMPFAN1	62	ACPI - 3VSB / 5VDIMM		
33	FAN TYPE-K SYSFAN1/2	63	ATX Power - FrpntPanel / EMI		
34	FAN TYPE-K SYSFAN3/4	64	LED - EZDEBUG / AMP		
35	FAN GPIO NCT5605	65	LED - DIMM / PCIE SLOT		



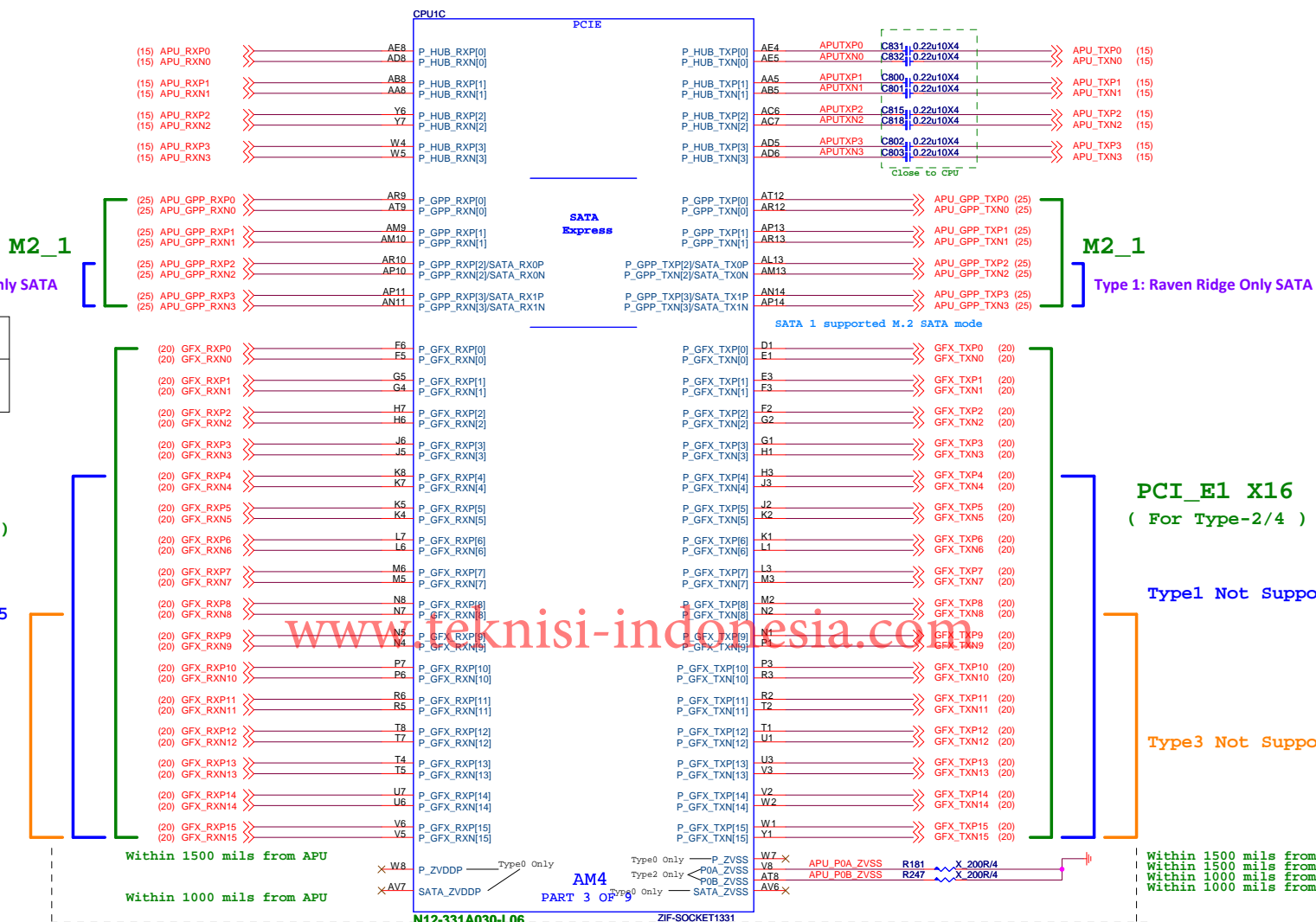


TYPE	PCIE	SATA
TYPE 0/1	2	2
TYPE 2/3/4	2 or 4	2 or 0

PCI\_E1 X16  
( For Type-2/4 )

Type1 Not Supported GFX 4~15

Type3 Not Support GFX 8~15





Date: Friday, April 26, 2019	Sheet 6 of 75
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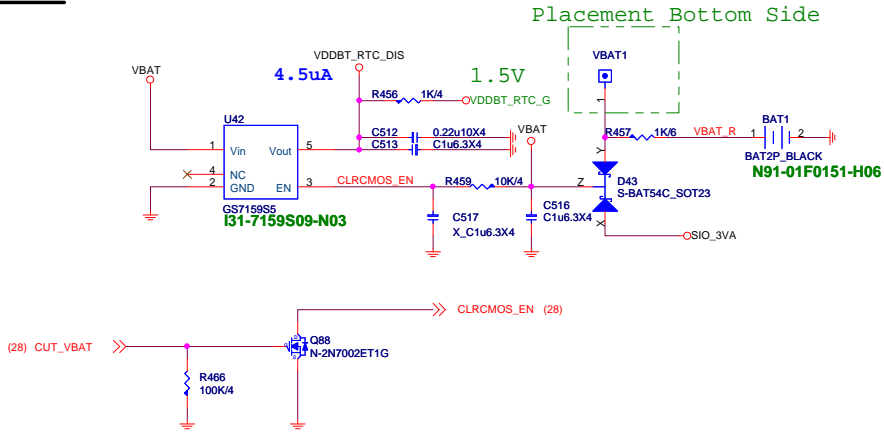


GND

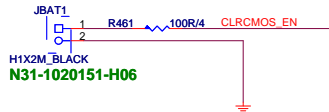
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AM4  
PART 9 OF 9

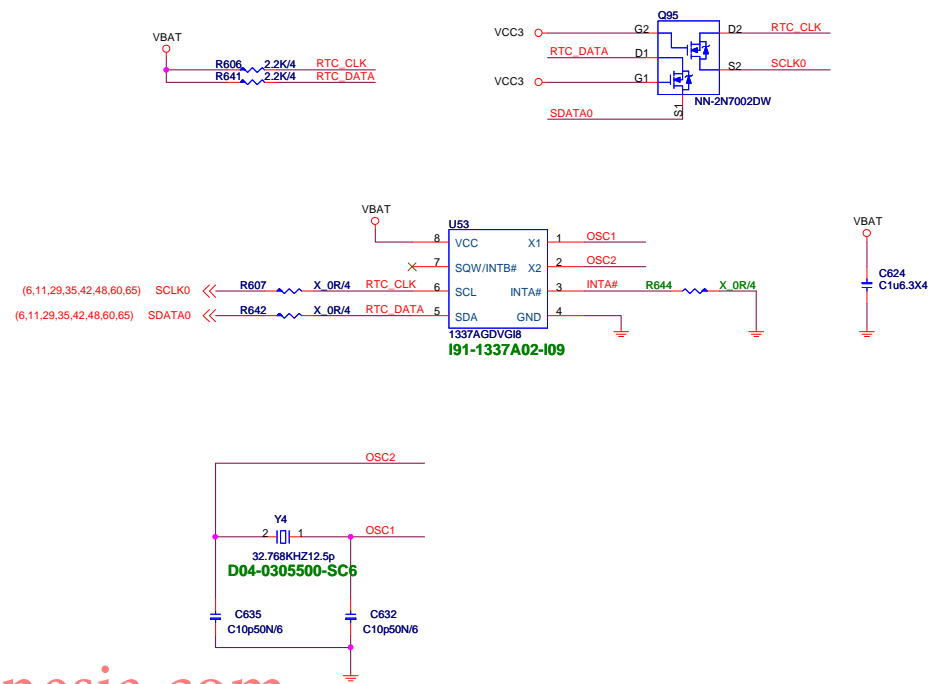
RTC & Clear CMOS Circuit



Clear CMOS button

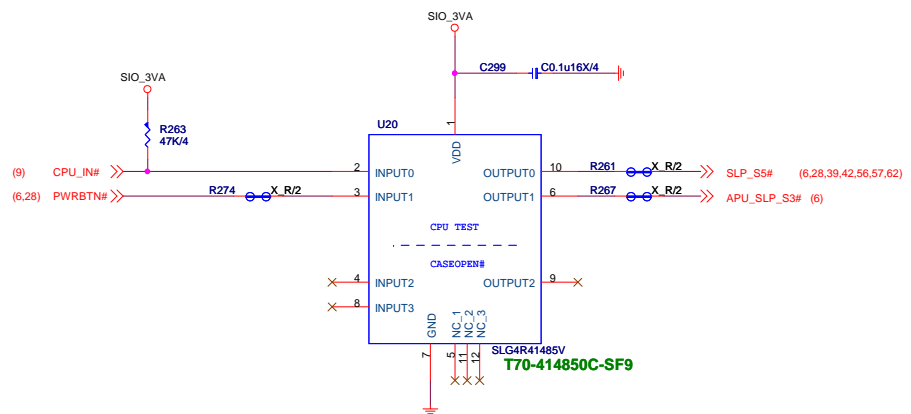


RTC Backup



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A1 A2 B1 B2

DIMMA1A

QDS17P 51  
QDS17N 52  
QDS16P 132  
QDS16N 133  
QDS15P 121  
QDS15N 122  
QDS14P 110  
QDS14N 111  
QDS13P 99  
QDS13N 100  
QDS12P 40  
QDS12N 41  
QDS11P 29  
QDS11N 30  
QDS10P 18  
QDS10N 19  
QDS9P 7  
QDS9N 8  
QDS8P 197  
QDS8N 198  
MA\_DQS\_H7 278  
MA\_DQS\_L7 277  
MA\_DQS\_H6 267  
MA\_DQS\_L6 266  
MA\_DQS\_H5 256  
MA\_DQS\_L5 255  
MA\_DQS\_H4 245  
MA\_DQS\_L4 244  
MA\_DQS\_H3 186  
MA\_DQS\_L3 185  
MA\_DQS\_H2 175  
MA\_DQS\_L2 174  
MA\_DQS\_H1 164  
MA\_DQS\_L1 163  
MA\_DQS\_H0 153  
MA\_DQS\_L0 152  
MA\_CLK\_H1 218  
MA\_CLK\_L1 219  
MA\_CLK\_H0 74  
MA\_CLK\_L0 75  
C2 235  
S3\_N\_C1 237  
S2\_N\_C0 93  
MA0\_CS\_L1 89  
MA0\_CS\_L0 84  
MA0\_CKE1 203  
MA0\_CKE0 80  
MA0\_ODT1 91  
MA0\_ODT0 87  
CB-7 199  
CB-6 54  
CB-5 192  
CB-4 47  
CB-3 201  
CB-2 56  
CB-1 194  
CB-0 49  
RESET\_N 58  
EVENT\_N 78  
ALERT\_N 208  
ACT\_N 62  
PAR 222  
SAVE\_N\_NC 230  
RFU-0 144  
RFU-1 205  
RFU-2 227

DDRIV-288P\_BLACK  
N13-2880551-L06

DQ-63 280  
DQ-62 135  
DQ-61 128  
DQ-60 282  
DQ-59 137  
DQ-58 275  
DQ-57 130  
DQ-56 269  
DQ-55 124  
DQ-54 262  
DQ-53 117  
DQ-52 271  
DQ-51 126  
DQ-50 264  
DQ-49 119  
DQ-48 258  
DQ-47 113  
DQ-46 251  
DQ-45 106  
DQ-44 260  
DQ-43 115  
DQ-42 253  
DQ-41 108  
DQ-40 247  
DQ-39 102  
DQ-38 240  
DQ-37 95  
DQ-36 249  
DQ-35 104  
DQ-34 242  
DQ-33 97  
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DQ-30 181  
DQ-29 36  
DQ-28 190  
DQ-27 45  
DQ-26 183  
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DQ-23 32  
DQ-22 170  
DQ-21 25  
DQ-20 179  
DQ-19 34  
DQ-18 172  
DQ-17 27  
DQ-16 166  
DQ-15 21  
DQ-14 159  
DQ-13 14  
DQ-12 168  
DQ-11 23  
DQ-10 161  
DQ-9 16  
DQ-8 155  
DQ-7 10  
DQ-6 148  
DQ-5 157  
DQ-4 12  
DQ-3 150  
DQ-2 5  
DQ-1 5

BG-1 207  
BG-0 63  
BA-1 224  
BA-0 81  
A17 234  
A16\_RAS\_N 82  
A15\_CAS\_N 86  
A14\_WE\_N 228  
A13 65  
A12 210  
A11 225  
A10 66  
A9 68  
A8 211  
A7 69  
A6 213  
A5 214  
A4 71  
A3 216  
A2 72  
A1 79  
A0 79

SCL  
SDASA-2  
SA-1  
SA-0DIMM1 (CHANNEL-A) -A0  
ADDRESS = 0:0 [SA1:SA0]

&lt;&lt; MA\_DATA[63..0] (3)

56-63

48-55

40-47

32-39

24-31

16-23

8-15

0-7

BG-1 207  
BG-0 63  
BA-1 224  
BA-0 81A17 234  
A16\_RAS\_N 82  
A15\_CAS\_N 86  
A14\_WE\_N 228  
A13 65  
A12 210  
A11 225  
A10 66  
A9 68  
A8 211  
A7 69  
A6 213  
A5 214  
A4 71  
A3 216  
A2 72  
A1 79  
A0 79SCL  
SDASA-2  
SA-1  
SA-0DIMM1 (CHANNEL-A) -A0  
ADDRESS = 0:0 [SA1:SA0]

SMBus 0	
Device	8-bit Address (hex)
DIMMA0	A0
DIMMA1	A4
DIMMB0	A2
DIMMB1	A6

VCC\_DDR

R186

1K/4

MA\_RESET\_L 58  
MA\_EVENT\_L 78  
MA\_ALERT\_L 208  
MA\_ACT\_L 62  
MA\_PAROUT 222SAVE\_N\_NC 230  
RFU-0 144  
RFU-1 205  
RFU-2 227

DIMMA2A

QDS17P 51  
QDS17N 52  
QDS16P 132  
QDS16N 133  
QDS15P 121  
QDS15N 122  
QDS14P 110  
QDS14N 111  
QDS13P 99  
QDS13N 100  
QDS12P 40  
QDS12N 41  
QDS11P 29  
QDS11N 30  
QDS10P 18  
QDS10N 19  
QDS9P 7  
QDS9N 8  
QDS8P 197  
QDS8N 198  
MA\_DQS\_H7 278  
MA\_DQS\_L7 277  
MA\_DQS\_H6 267  
MA\_DQS\_L6 266  
MA\_DQS\_H5 256  
MA\_DQS\_L5 255  
MA\_DQS\_H4 245  
MA\_DQS\_L4 244  
MA\_DQS\_H3 186  
MA\_DQS\_L3 185  
MA\_DQS\_H2 175  
MA\_DQS\_L2 174  
MA\_DQS\_H1 164  
MA\_DQS\_L1 163  
MA\_DQS\_H0 153  
MA\_DQS\_L0 152  
MA\_CLK\_H3 218  
MA\_CLK\_L3 219  
MA\_CLK\_H2 74  
MA\_CLK\_L2 75  
C2 235  
S3\_N\_C1 237  
S2\_N\_C0 93  
MA1\_CS\_L1 89  
MA1\_CS\_L0 84  
MA1\_CKE1 203  
MA1\_CKE0 80  
MA1\_ODT1 91  
MA1\_ODT0 87  
CB-7 199  
CB-6 54  
CB-5 192  
CB-4 47  
CB-3 201  
CB-2 56  
CB-1 194  
CB-0 49  
RESET\_N 58  
EVENT\_N 78  
ALERT\_N 208  
ACT\_N 62  
PAR 222  
SAVE\_N\_NC 230  
RFU-0 144  
RFU-1 205  
RFU-2 227

DDRIV-288P\_BLACK  
N13-2880551-L06

DQ-63 280  
DQ-62 135  
DQ-61 128  
DQ-60 282  
DQ-59 137  
DQ-58 275  
DQ-57 130  
DQ-56 269  
DQ-55 124  
DQ-54 262  
DQ-53 117  
DQ-52 271  
DQ-51 126  
DQ-50 264  
DQ-49 119  
DQ-48 258  
DQ-47 113  
DQ-46 251  
DQ-45 106  
DQ-44 260  
DQ-43 115  
DQ-42 253  
DQ-41 108  
DQ-40 247  
DQ-39 102  
DQ-38 240  
DQ-37 95  
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DQ-28 190  
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DQ-24 177  
DQ-23 32  
DQ-22 170  
DQ-21 25  
DQ-20 179  
DQ-19 34  
DQ-18 172  
DQ-17 27  
DQ-16 166  
DQ-15 21  
DQ-14 159  
DQ-13 14  
DQ-12 168  
DQ-11 23  
DQ-10 161  
DQ-9 16  
DQ-8 155  
DQ-7 10  
DQ-6 148  
DQ-5 157  
DQ-4 12  
DQ-3 150  
DQ-2 5  
DQ-1 5

BG-1 207  
BG-0 63  
BA-1 224  
BA-0 81A17 234  
A16\_RAS\_N 82  
A15\_CAS\_N 86  
A14\_WE\_N 228  
A13 65  
A12 210  
A11 225  
A10 66  
A9 68  
A8 211  
A7 69  
A6 213  
A5 214  
A4 71  
A3 216  
A2 72  
A1 79  
A0 79SCL  
SDASA-2  
SA-1  
SA-0DIMM2 (CHANNEL-A) -A4  
ADDRESS = 1:0 [SA1:SA0]

&lt;&lt; MA\_DATA[63..0] (3)

56-63

48-55

40-47

32-39

24-31

16-23

8-15

0-7

BG-1 207  
BG-0 63  
BA-1 224  
BA-0 81A17 234  
A16\_RAS\_N 82  
A15\_CAS\_N 86  
A14\_WE\_N 228  
A13 65  
A12 210  
A11 225  
A10 66  
A9 68  
A8 211  
A7 69  
A6 213  
A5 214  
A4 71  
A3 216  
A2 72  
A1 79  
A0 79SCL  
SDASA-2  
SA-1  
SA-0DIMM2 (CHANNEL-A) -A4  
ADDRESS = 1:0 [SA1:SA0]

VCC3\_SPD\_A2A1

R303

1K/4

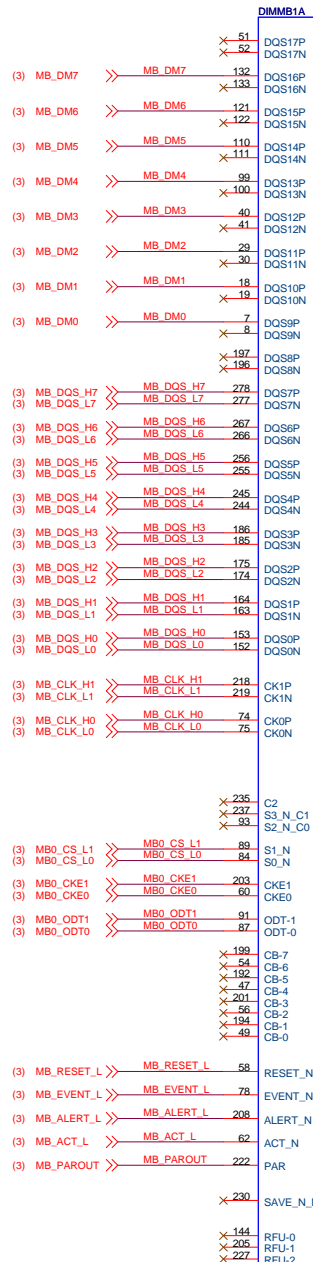
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MA\_EVENT\_L 78  
MA\_ALERT\_L 208  
MA\_ACT\_L 62  
MA\_PAROUT 222SAVE\_N\_NC 230  
RFU-0 144  
RFU-1 205  
RFU-2 227

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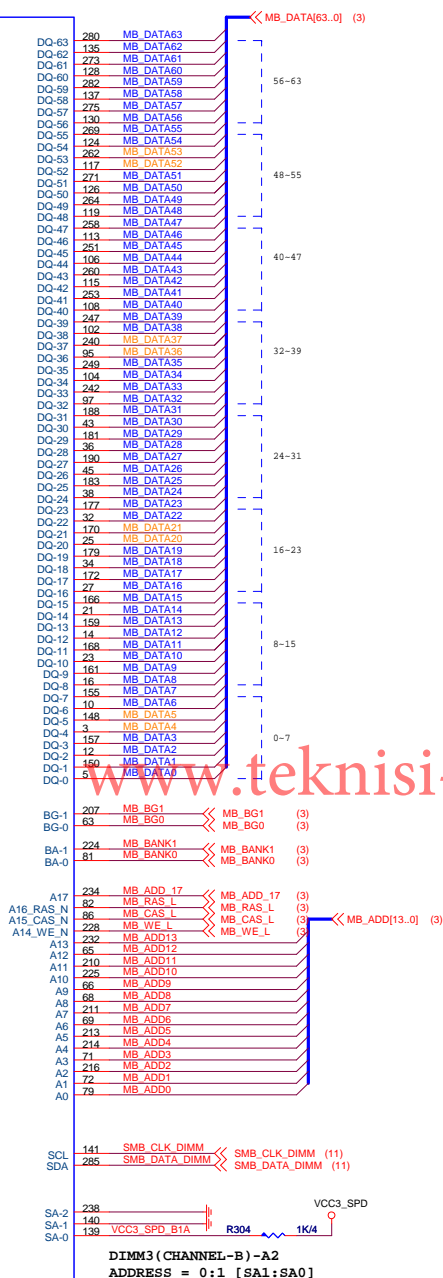
MS-7C37

Size	Document Description	Rev
Custom	DDR4 - DIMM CH-A	2.1
Date: Friday, April 26, 2019		
Sheet 11 of 75		

(6,10,29,35,42,48,60,65) SCLK0 SCLK0 R333 X R/2 SMB\_CLK\_DIMM (12)  
(6,10,29,35,42,48,60,65) SDATA0 SDATA0 R328 X R/2 SMB\_DATA\_DIMM (12)



DDRIV-288P\_BLACK  
N13-2880551-L06



DIMM3 (CHANNEL-B) -A2  
ADDRESS = 0:1 [SA1:SA0]



DDRIV-288P\_BLACK  
N13-2880551-L06

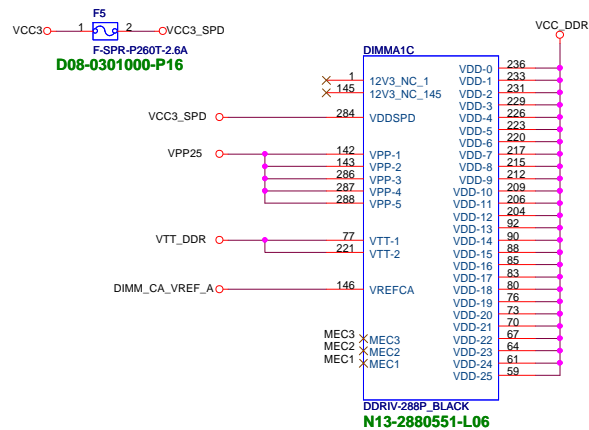


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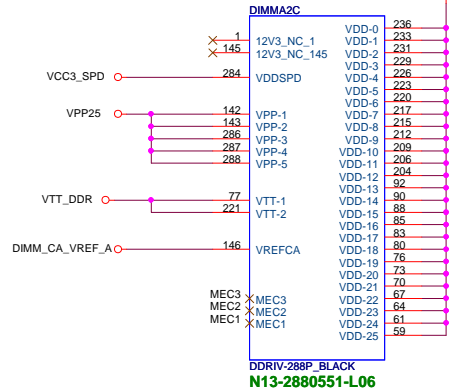
MS-7C37

Size	Document Description	Rev
Custom	DDR4 - DIMM CH-B	2.1
Date: Friday, April 26, 2019		Sheet 12 of 75

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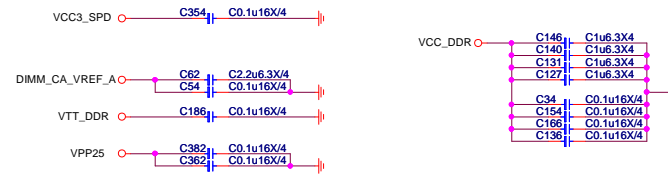
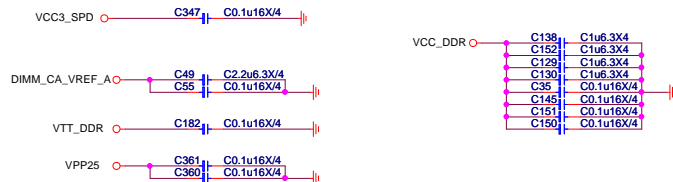
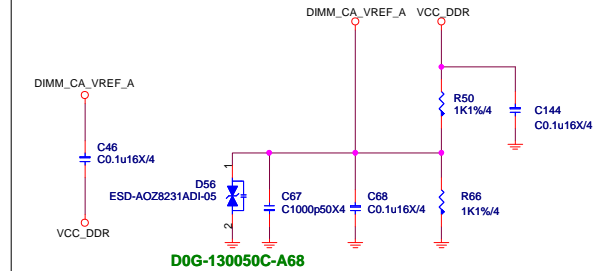


DIMM SLOT PN BY SPEC

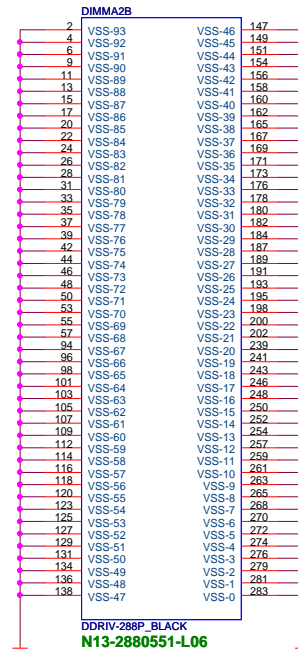
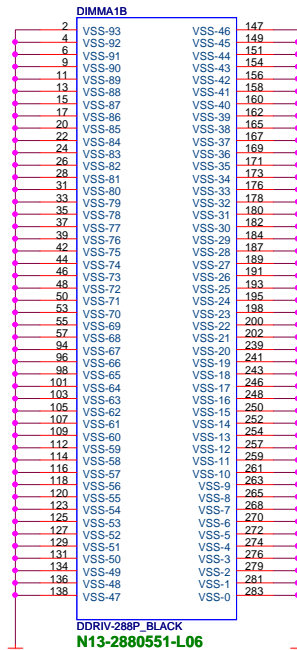


## DDR VREF

(place resistors close to DIMMs)



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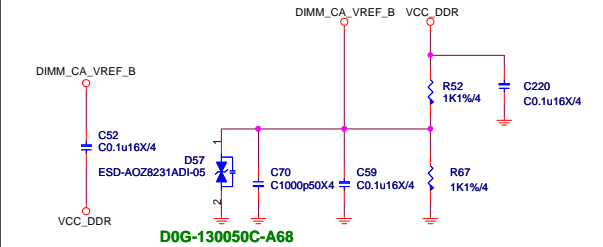
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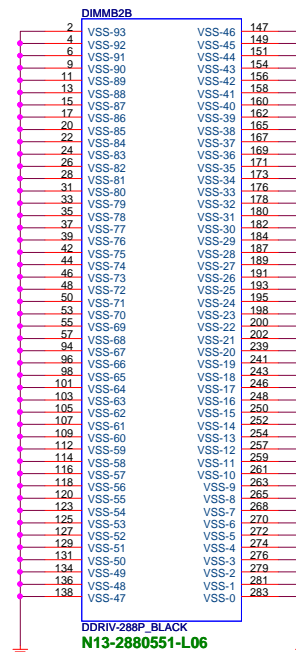
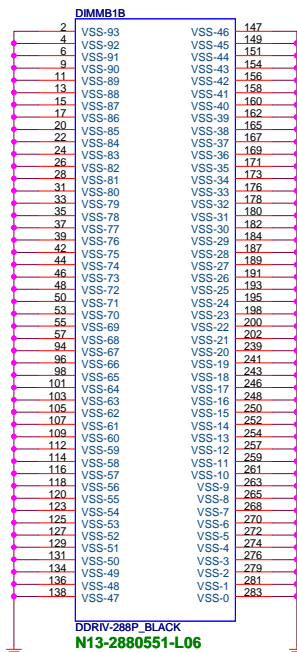
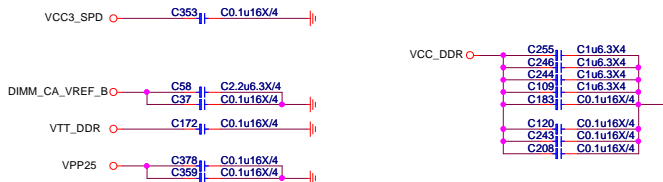
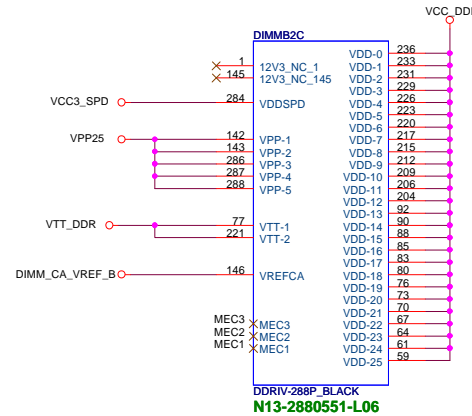
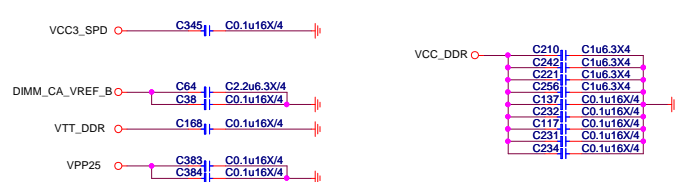
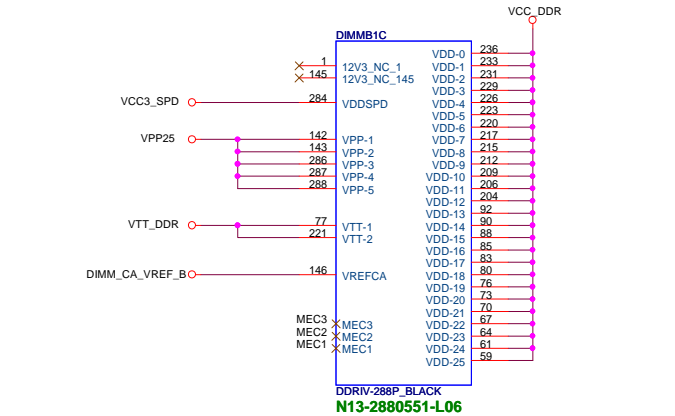
Size	Document Description	Rev
Custom	DDR4 - POWER/GND-1	2.1
Date:	Tuesday, April 23, 2019	Sheet 13 of 75

# DDR VREF

(place resistors close to DIMMs)

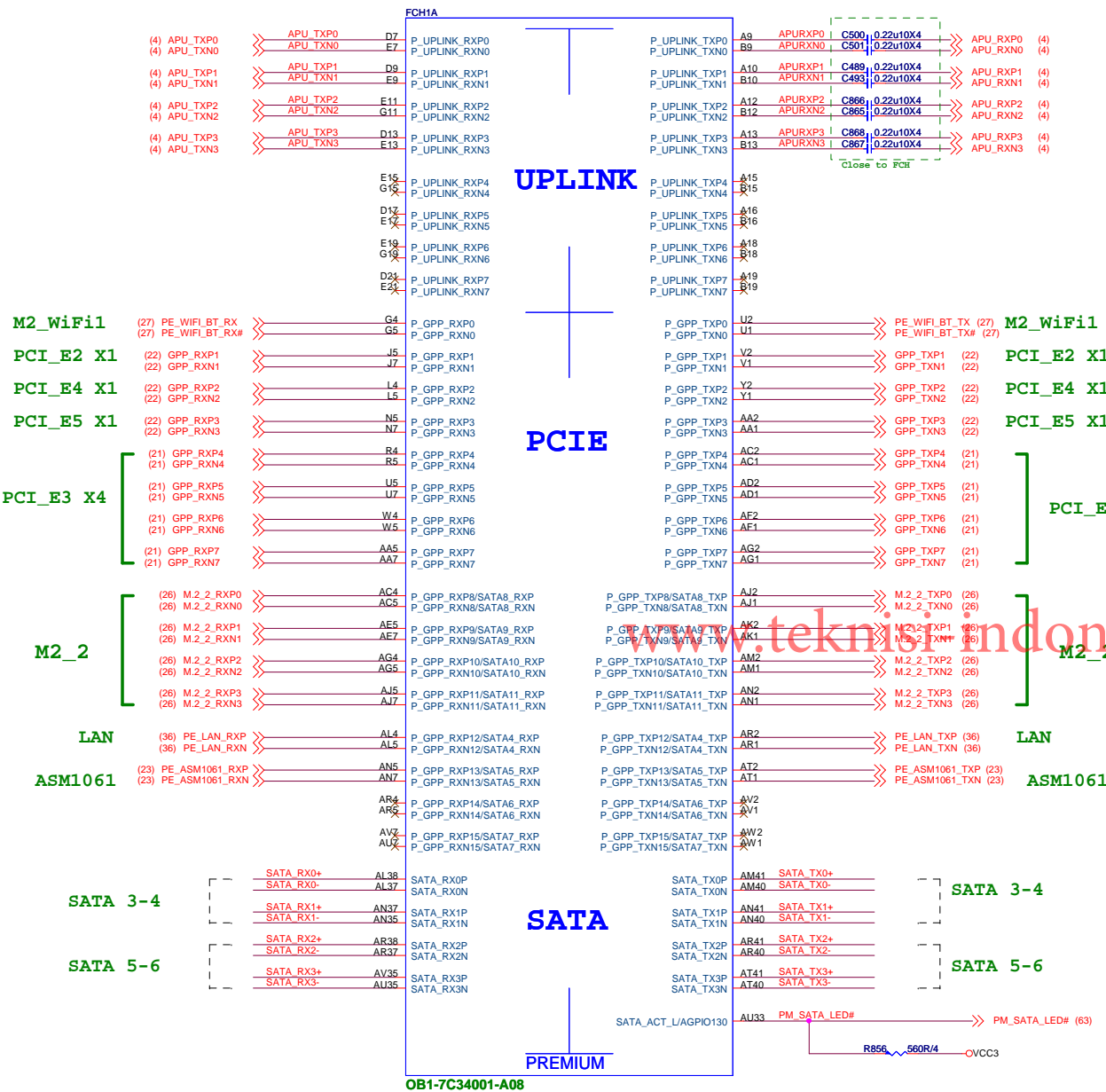
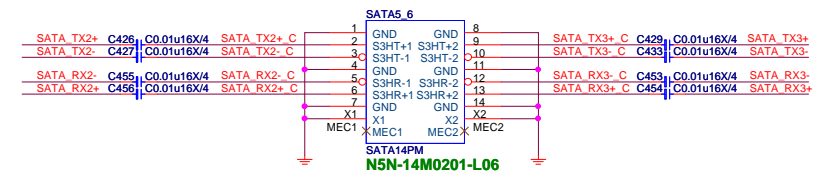
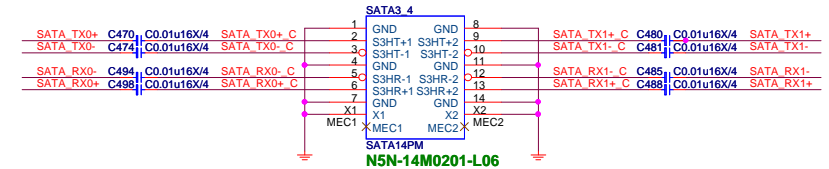


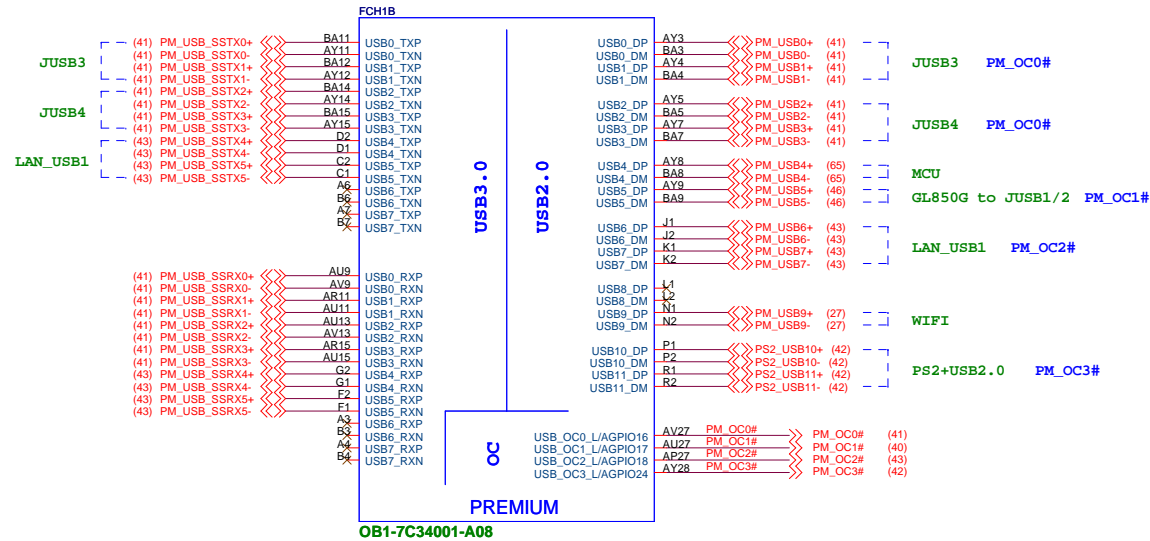
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## SATA Connector



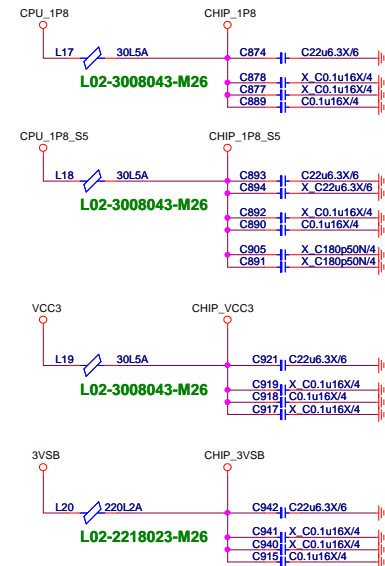
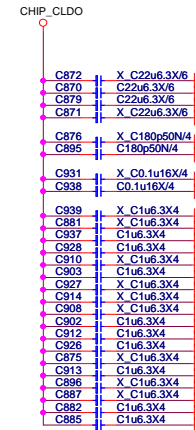
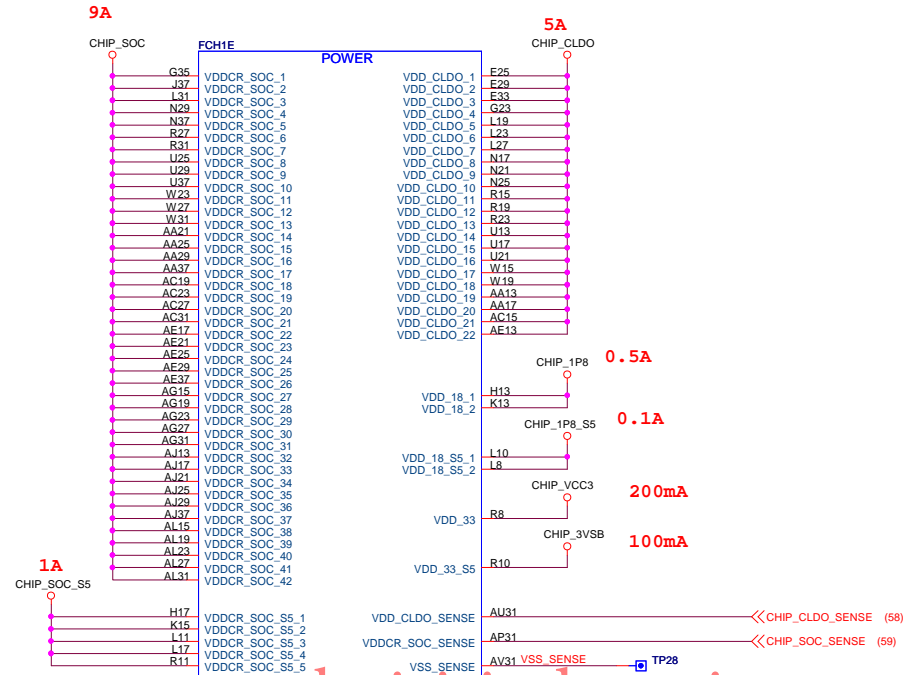
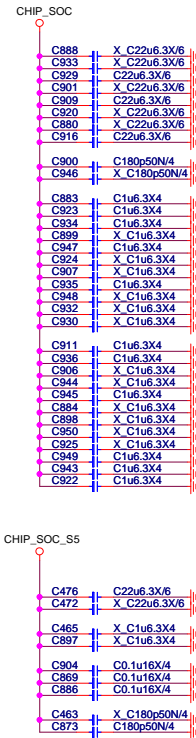


Ports	Host Controller	OC Pins Mapped
USB 3.2 Port 0 - 3 and USB 2.0 Port 0 - 5	Host Controller 0 (HC0)	USB_OC0_L/AGPIO16 USB_OC1_L/AGPIO17
USB 3.2 Port 4 - 7 and USB 2.0 Port 6 - 11	Host Controller 1 (HC1)	USB_OC2_L/AGPIO18 USB_OC3_L/AGPIO24

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PREMIUM

OB1-7C34001-A08

GND

PREMIUM [www.teknisi-indonesia.com](http://www.teknisi-indonesia.com)

teknisi indonesia



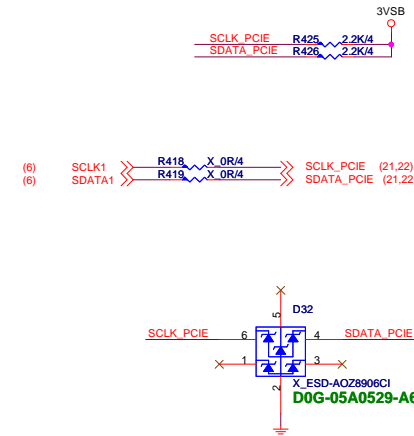
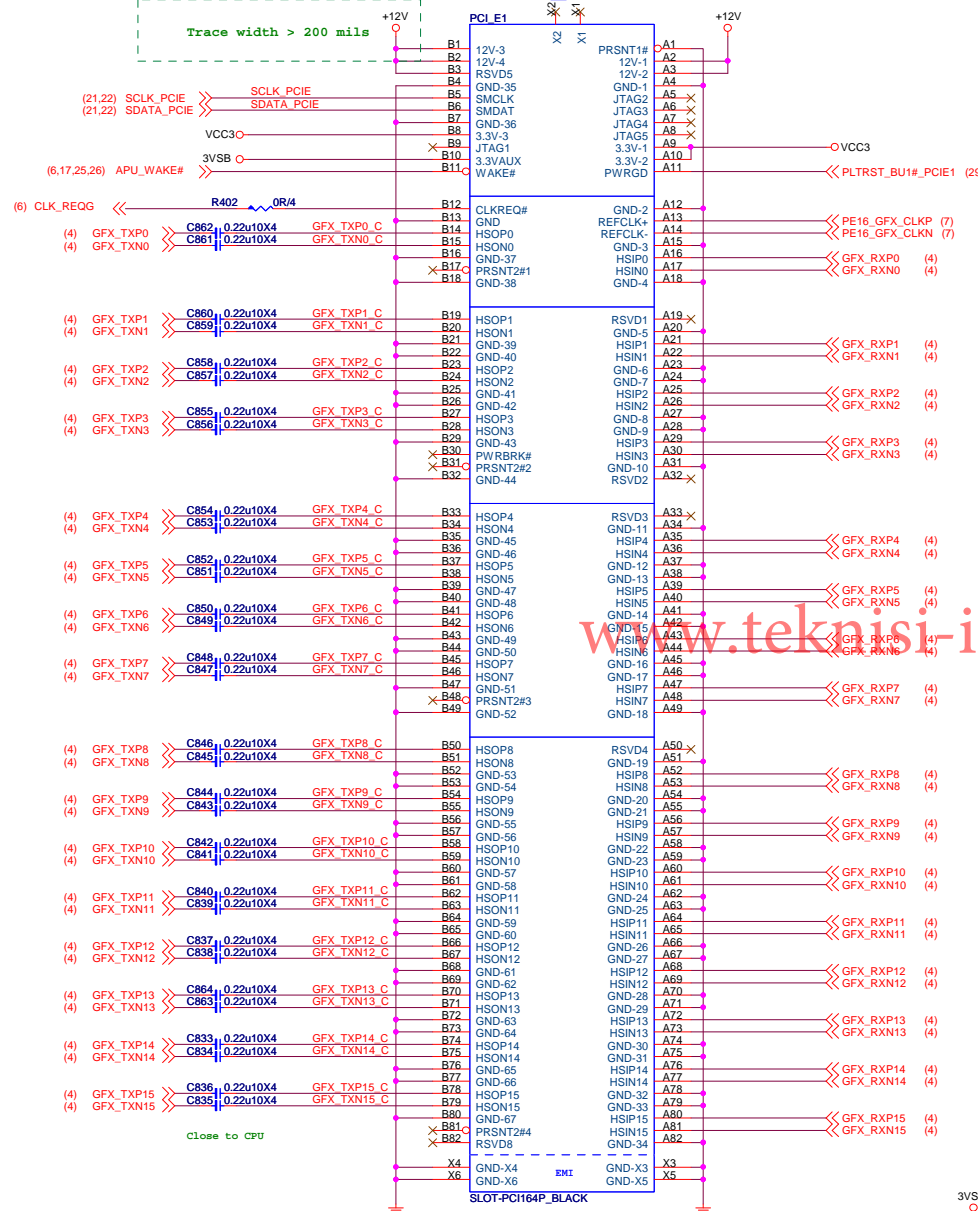
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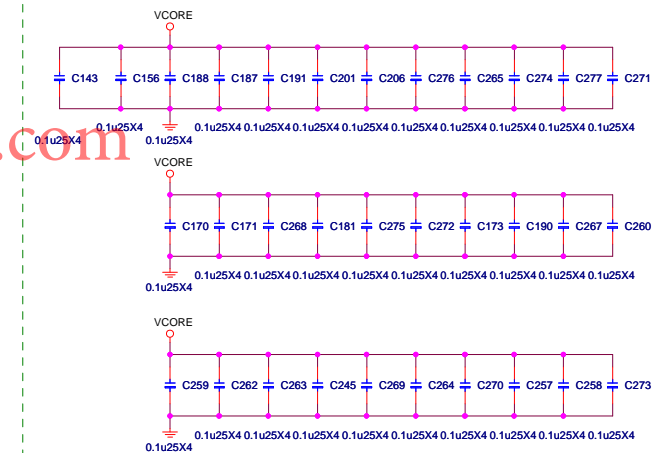
Size	Document Description	Rev
Custom	Premium - GND	2.1
Date: Tuesday, April 23, 2019		Sheet 19 of 75

# PCI EXPRESS x16 Slot

## PCI E1



## Bypass Capacitor For Across Moat



## PCI Express x16 Slot

+12V	- 5.5A
+VCC3	- 3A
+3V3_S5 (wake)	- 375mA
+3V3_S5 (no wake)	- 20mA



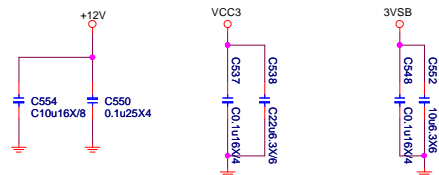
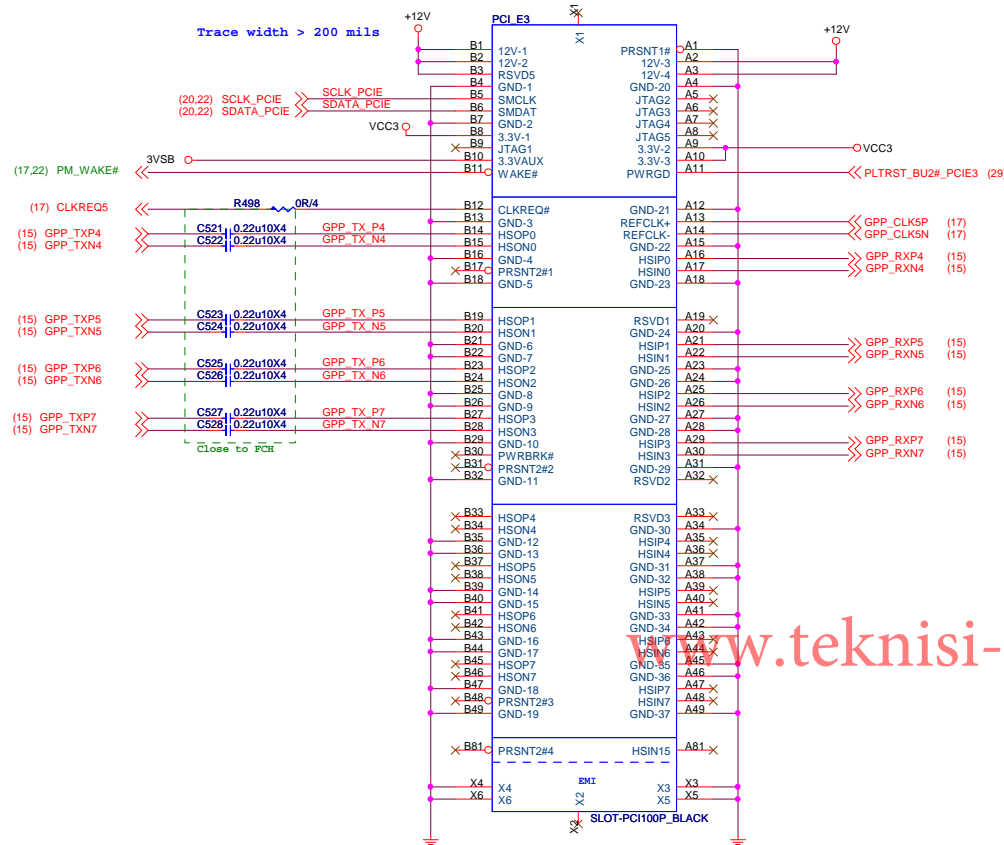
MICRO-STAR INT'L CO.,LTD

MS-7C37

Size	Document Description	Rev
Custom	PCI E1 (X16)	2.1
Date: Friday, April 26, 2019	Sheet 20 of 75	



## PCI\_E3 X4



### PCI Express x4 Slot \*1

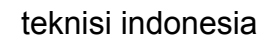
+12V	- 2.1A
+VCC3	- 3A
+3V3_S5 (wake)	- 375mA
+3V3_S5 (no wake)	- 20mA



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MS-7C37

Size	Document Description	Rev
Custom	PCI_E3 (X4)	2.1
Date: Friday, April 26, 2019	Sheet 21 of 75	



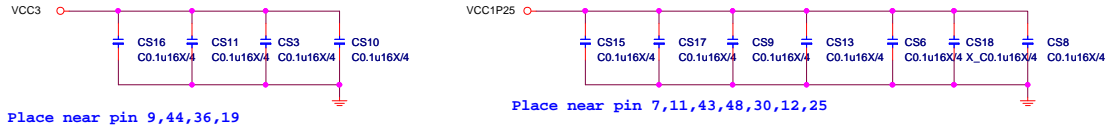
<b>MICRO-STAR INT'L CO.,LTD</b>			
<b>MS-7C37</b>			
Size Custom	Document Description		Rev 2.1
<b>PCIE Switch PCI_E2 / E4/ E5 (X1)</b>			
Date: Friday, April 26, 2019	Sheet	22	of 75

# SATA Connector

1.2V delay from 3.3V 90% > 0ms

ASM1061 POWER Consumption

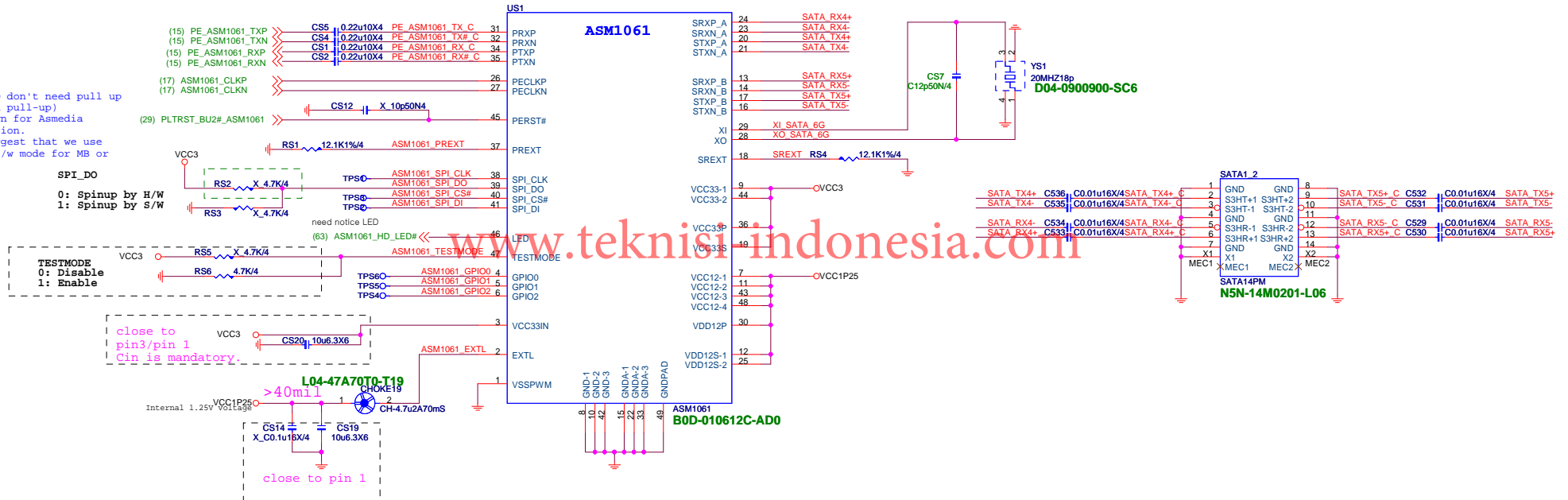
	3.3V	1.25V	Power (mW)
Idle (mA)	98.45	212.3	579.645
Busy (mA)	91.1	330.7	697.47




## ASM1061 SATA6G

SATA\_SPI\_DO don't need pull up (integrated pull-up) or pull down for Asmedia recommendation.  
Asmedia suggest that we use spinup by s/w mode for MB or PCI-E Card.

SPI\_DO  
0: Spinup by H/W  
1: Spinup by S/W

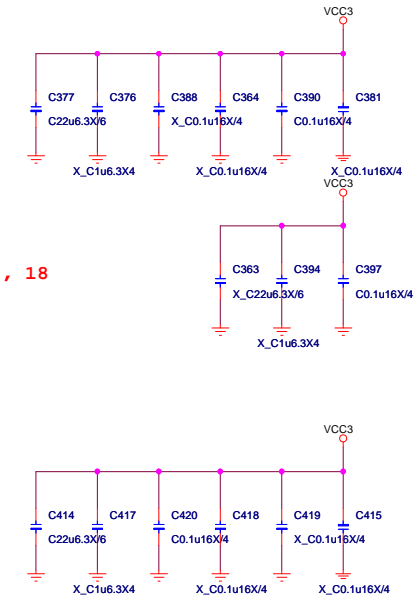
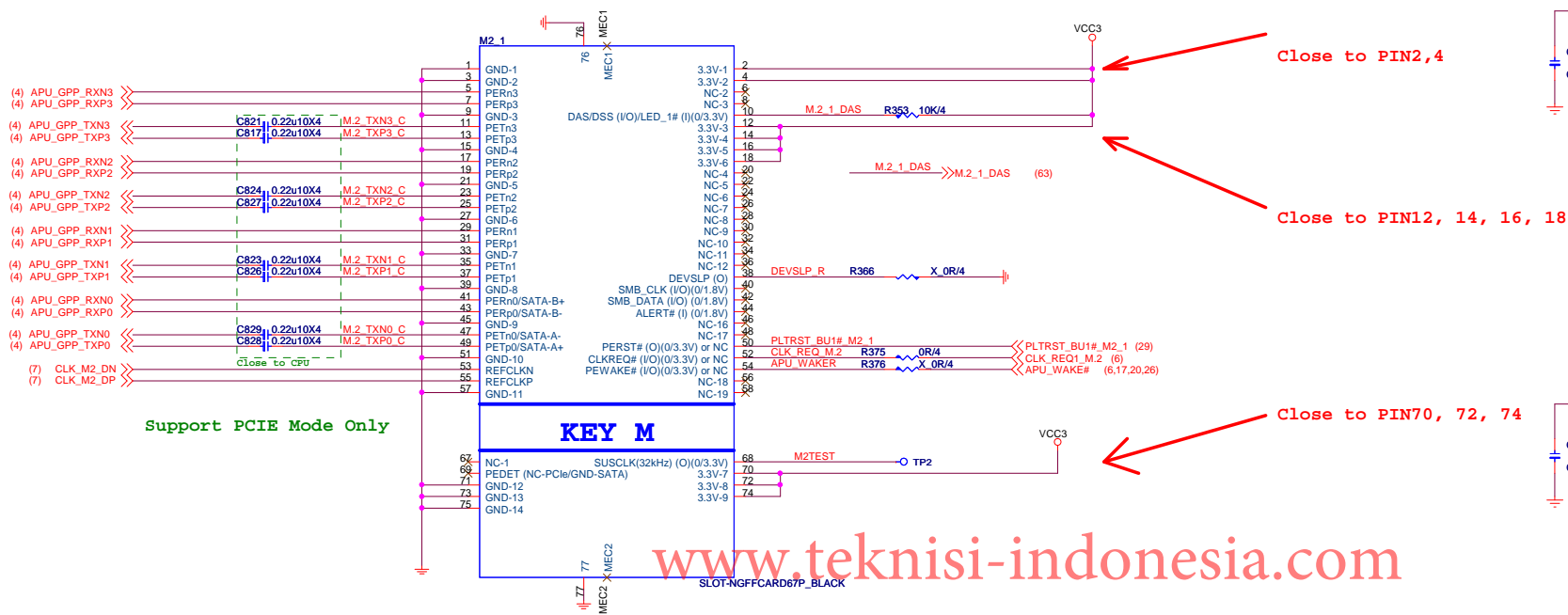


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			<b>MICRO-STAR INT'L CO.,LTD</b>	
			<b>MS-7C37</b>	
Size Custom	Document Description <b>PCI_E1_E3_E5 (X1)</b>			Rev 2.1
Date: Tuesday, April 23, 2019		Sheet 24 of 75		

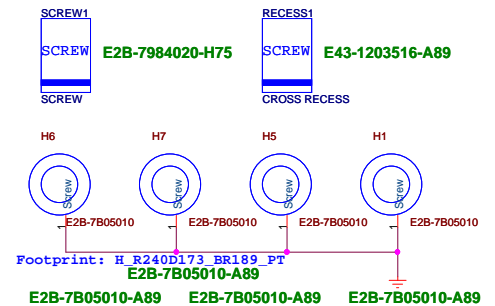
## M.2 1 Connector

VCC3 4.25A  
Max: 14W



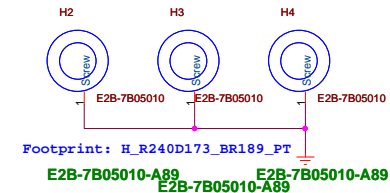
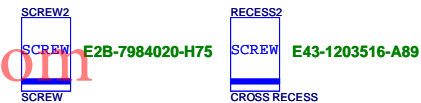
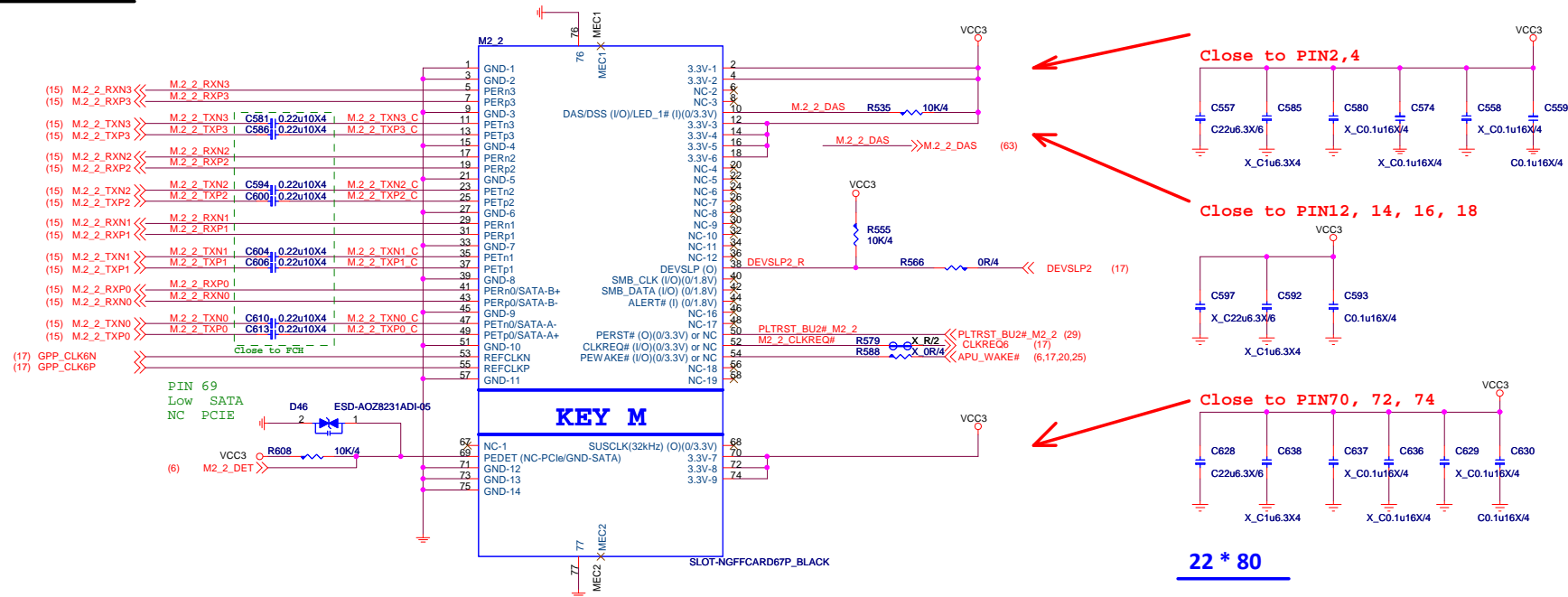
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22 \* 110

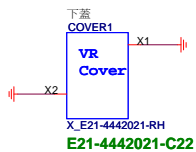
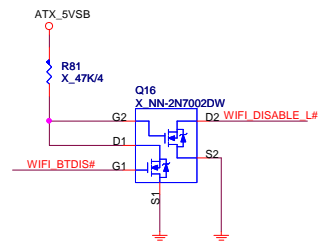
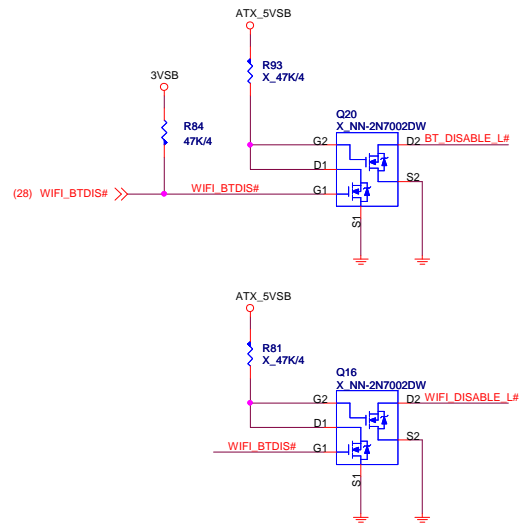
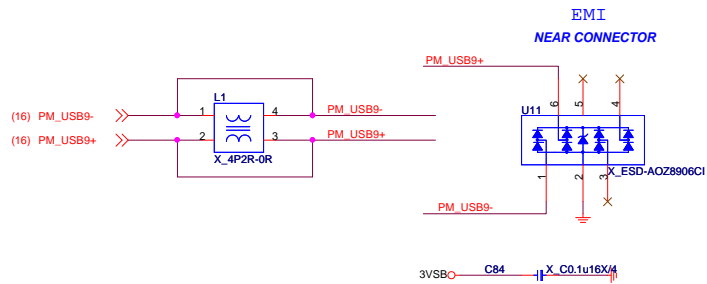


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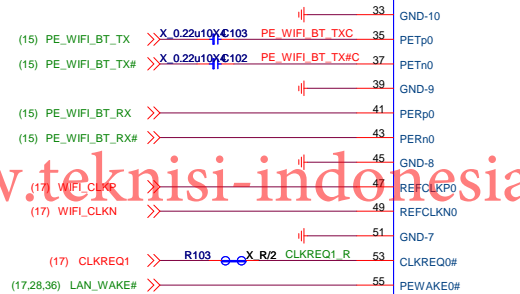
## M.2 2 Connector





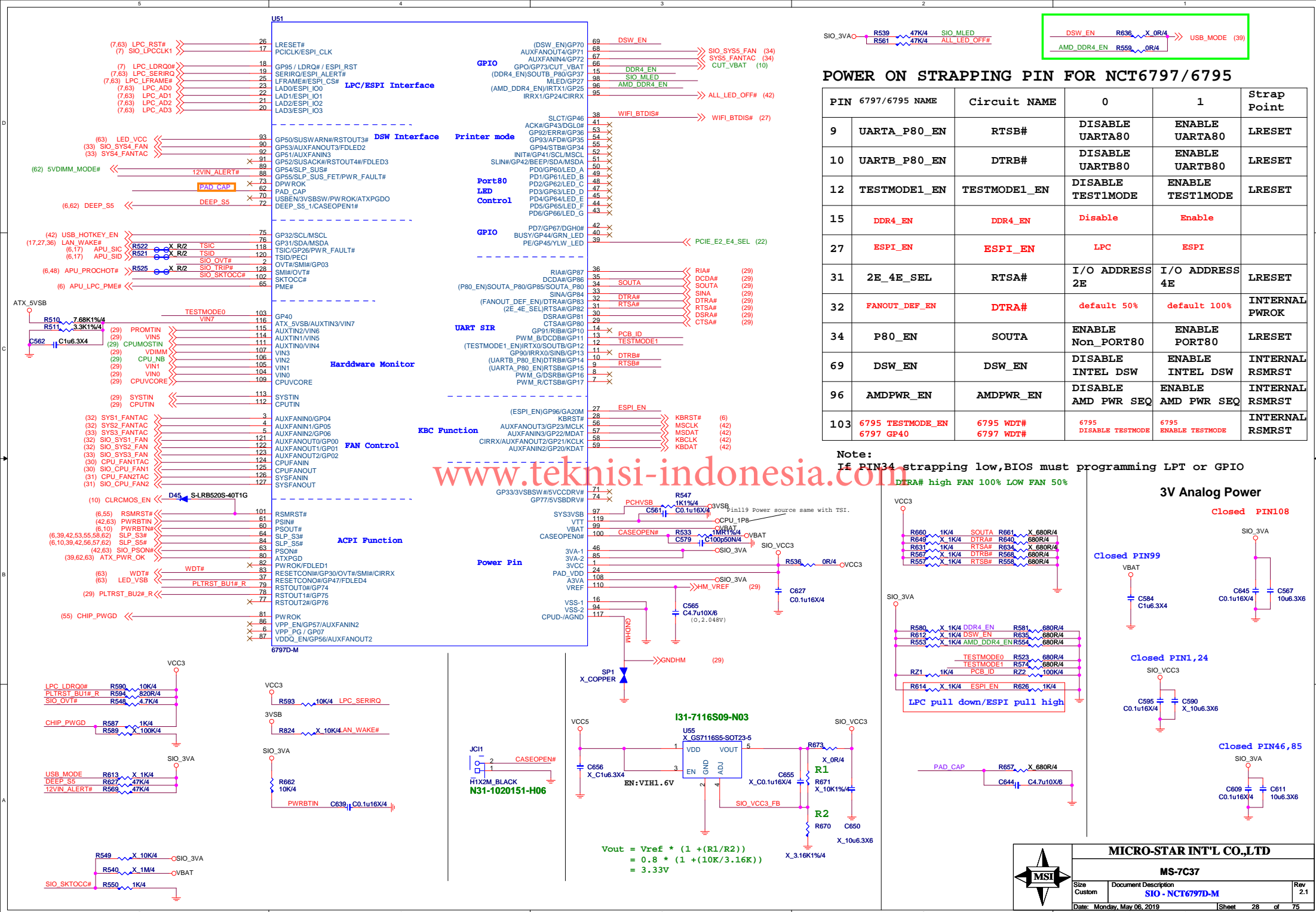


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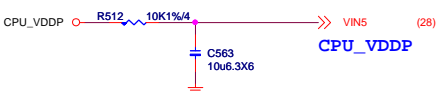
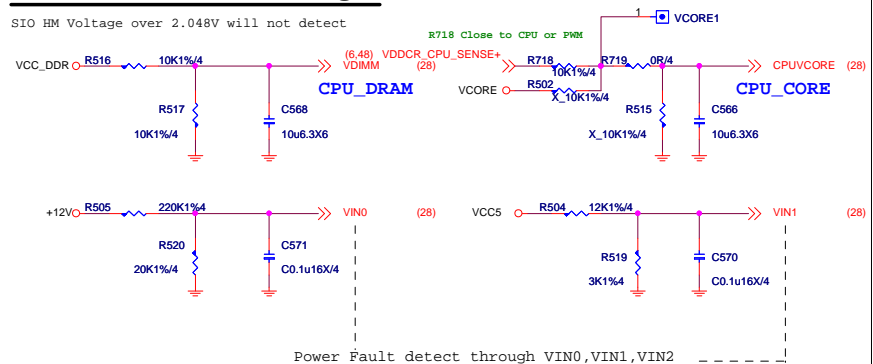
N15-0670610-L06

10uP+0.1uP+0.01uP at one end of socket in support of 3.3 V3V pins 2 and 4.  
10uP+0.1uP+0.01uP at the other end of the socket in support of 3.3 V3V pins 70 and 72.

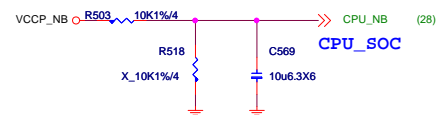


# HW Monitor - Voltage

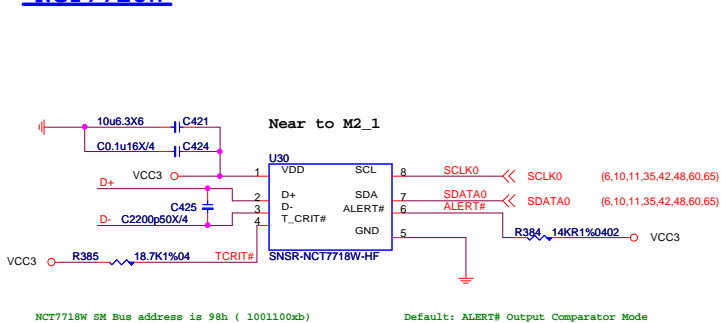
SIO HM Voltage over 2.048V will not detect



Inform BIOS disable VIN2 with Power Fault



## NCT7718W



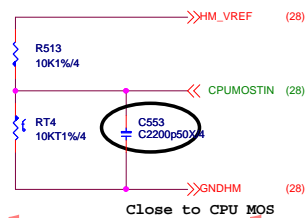
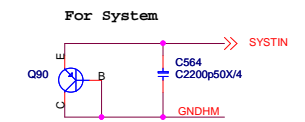
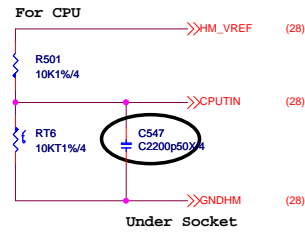
NCT7718W SM Bus address is 98h ( 1001100xb)

Default: ALERT# Output Comparator Mode

TEMPERATURE (°C)	T_CRIT#					
	2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ	
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

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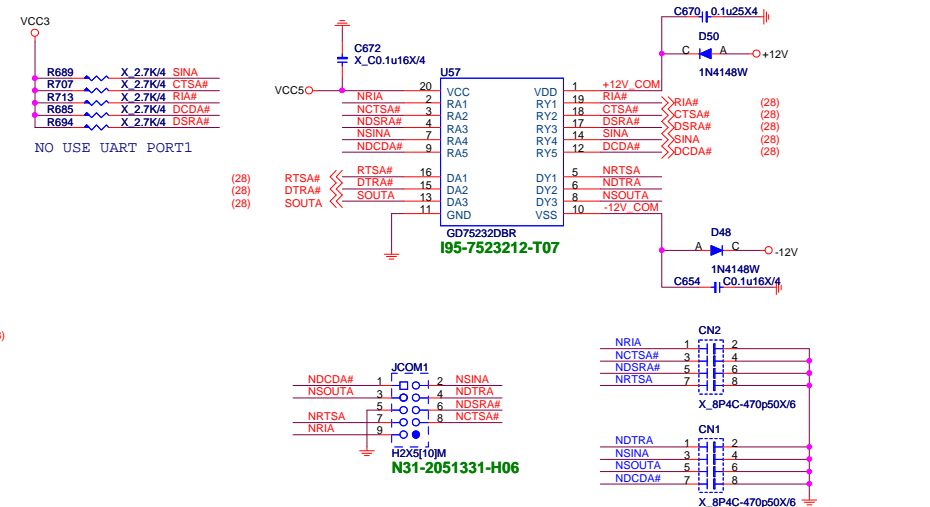
## TEMP SENSOR



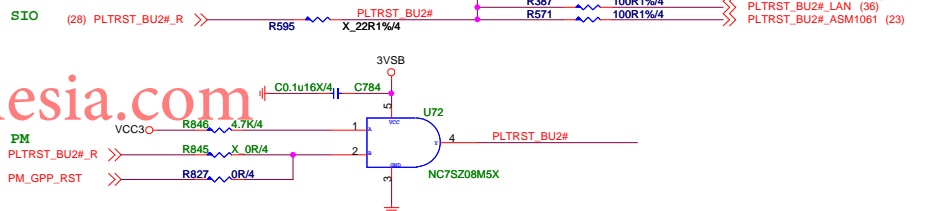
Close to CPU MOS

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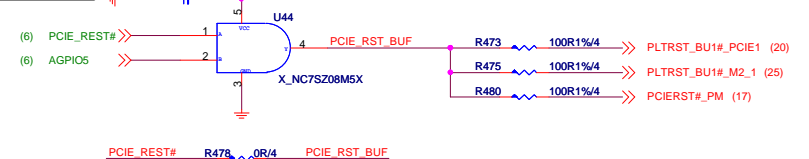
## COM PORT



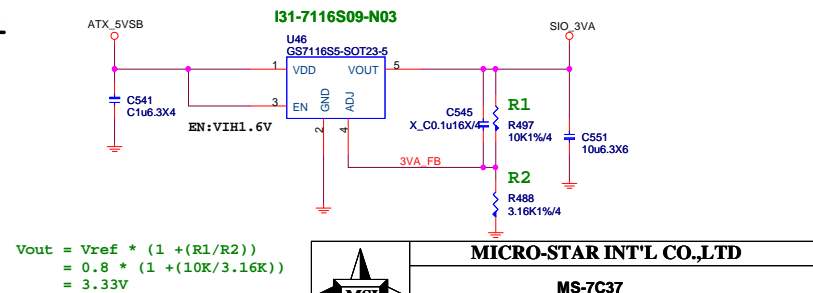
## PM RESET



## CPU RESET



## SIO\_3VA



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**MS-7C37**

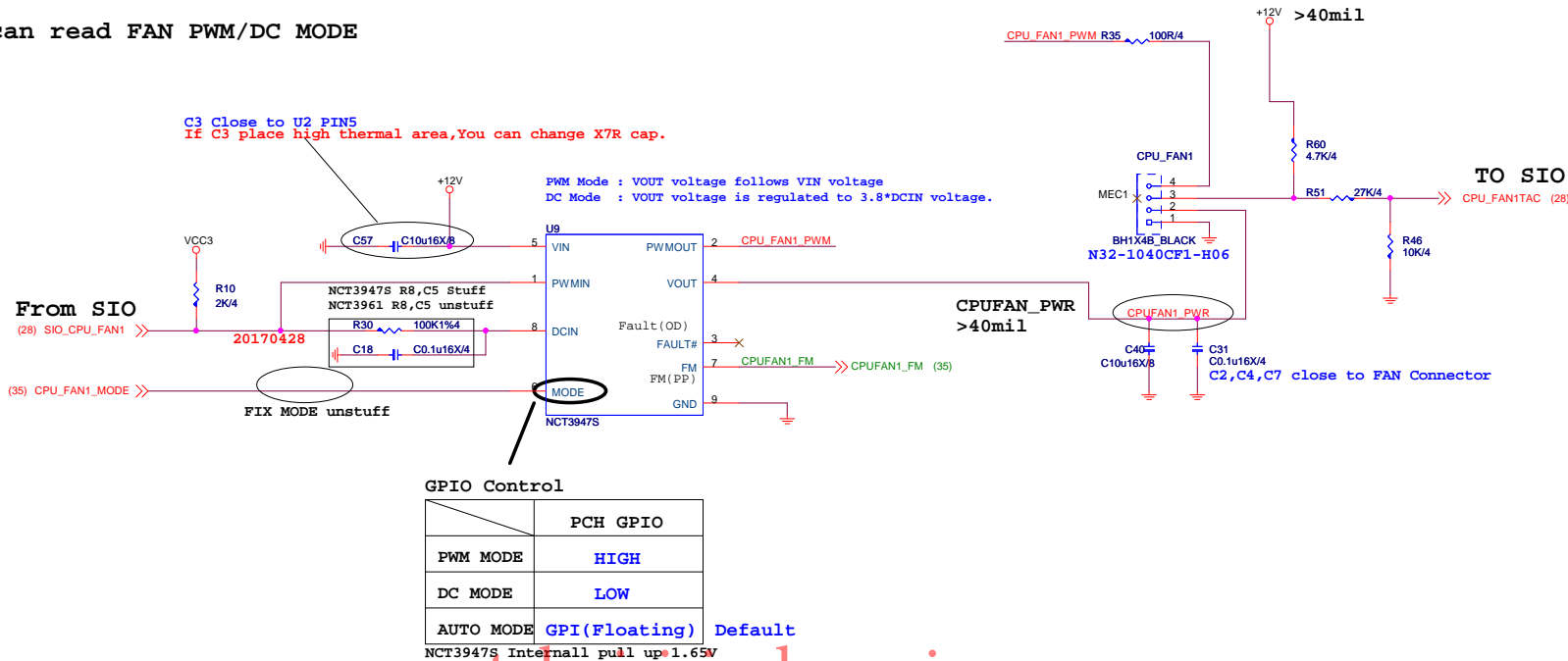
Size Custom Document Description **SIO - HW Monitor / NCT7718W** Rev 2.1

Date: Friday, April 26, 2019 Sheet 29 of 75

TYPE L : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO

CPUFAN1

- 1.Mode GPIO BIOS can swtich PWM/DC MODE
- 2.FM:BIOS can read FAN PWM/DC MODE

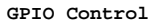


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## PUMPFAN1

## 1.Mode GPIO BIOS can swtich PWM/DC MODE



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

### Default

NCT3947S Internal pull up 1.65V



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MS-7C37

Size Custom	Document Description <b>FAN TYPE-K PUMPFANI</b>	Rev 2.1
Date: Friday, April 26, 2019	Sheet 31 of 75	

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

C3 Close to U2 PIN5  
If C3 place high thermal area, You can change X7R cap.

From SIO  
(28) SIO\_SYS1\_FAN >>>  
(35) SYS1\_FAN\_MODE >>>

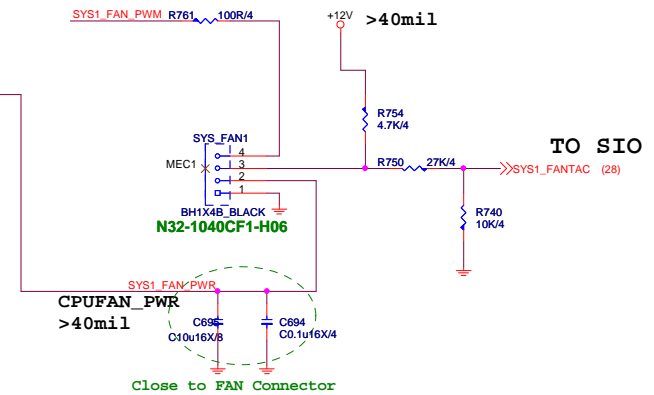
20170428

FIX MODE unstuff

GPIO Control

	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

Internall pull up 1.65V



TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

C3 Close to U2 PIN5  
If C3 place high thermal area, You can change X7R cap.

PWM Mode : VOUT voltage follows VIN voltage  
DC Mode : VOUT voltage is regulated to 3.8\*DCIN voltage.

C3 Close to U1 PIN5

From SIO  
(28) SIO\_SYS2\_FAN >>

(35) SYS2\_FAN\_MODE >>

VCC3  
R696 2K/4

NCT3947S R8,C5 Stuff  
NCT3961 R8,C5 unstuff

R697 100K1%  
C685 C0.1u16X4

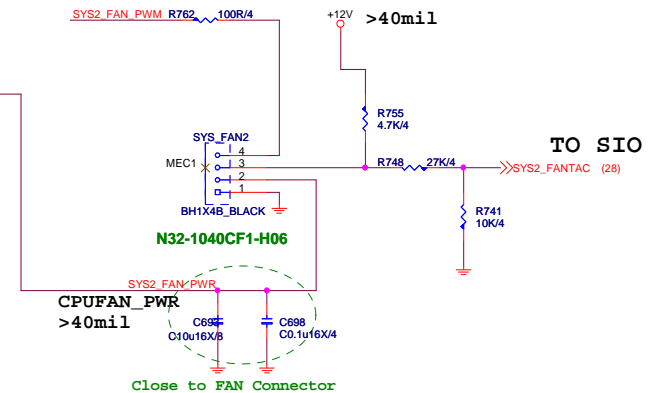
20170428

FIX MODE unstuff

GPIO Control

	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V



MS-7C37

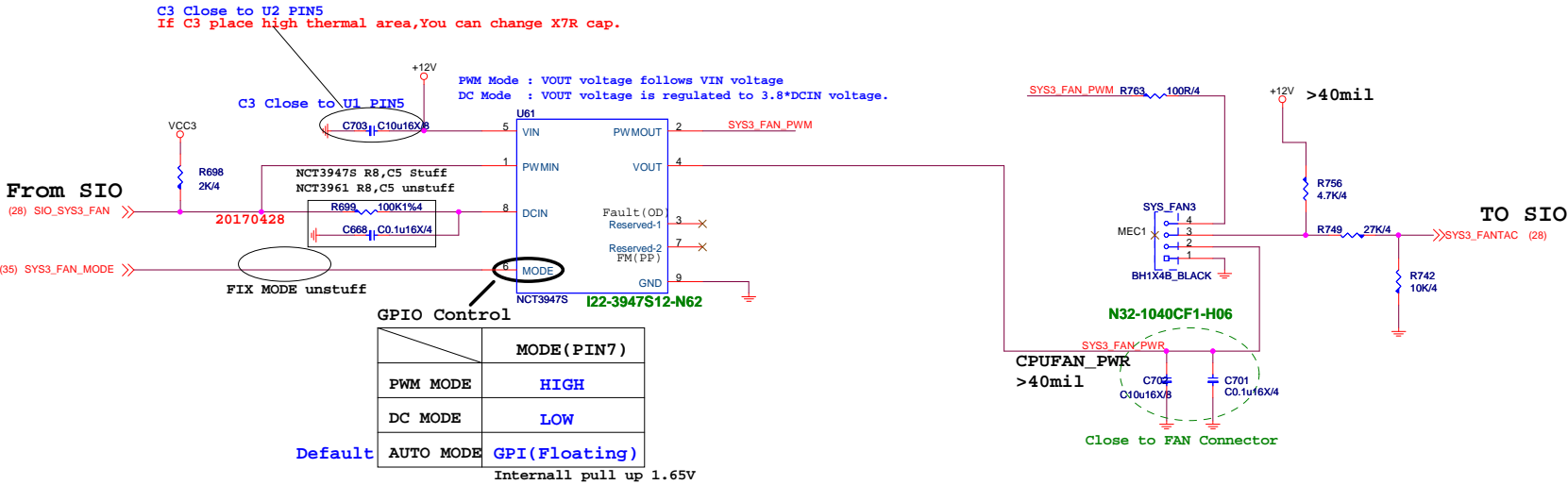
Size Custom	Document Description <b>FAN TYPE-K SYSFANI/2</b>	Rev 2.1
Date: Friday, April 26, 2019		Sheet 32 of 75



SYSFAN3

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

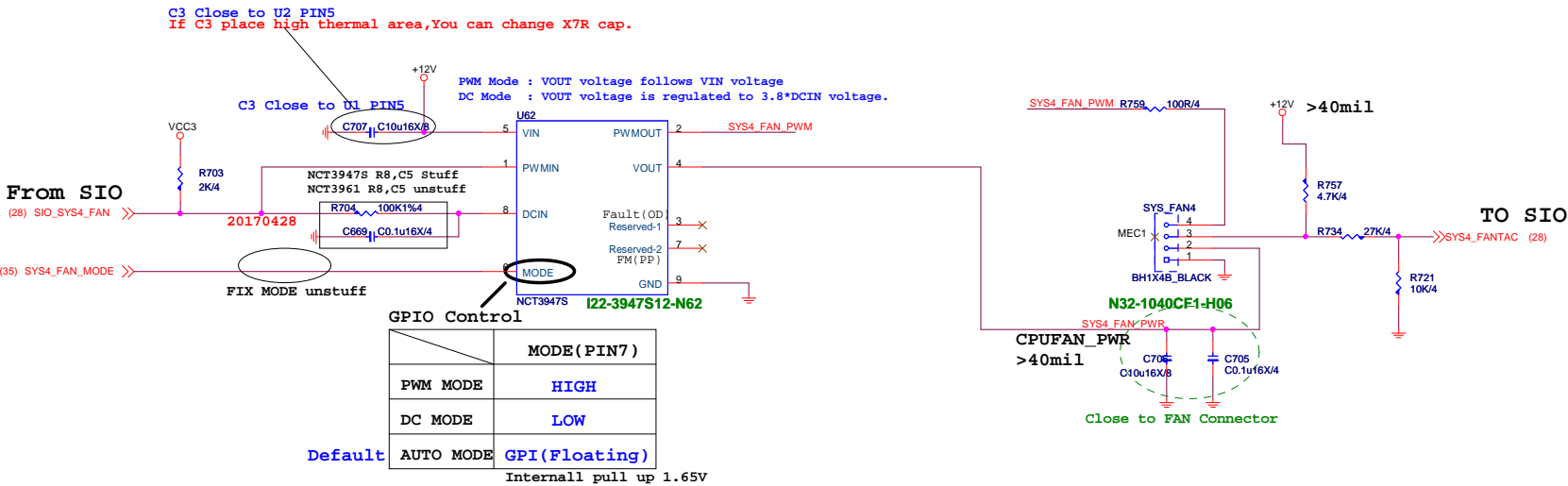
1.Mode GPIO BIOS can swtich PWM/DC MODE



SYSFAN4

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE

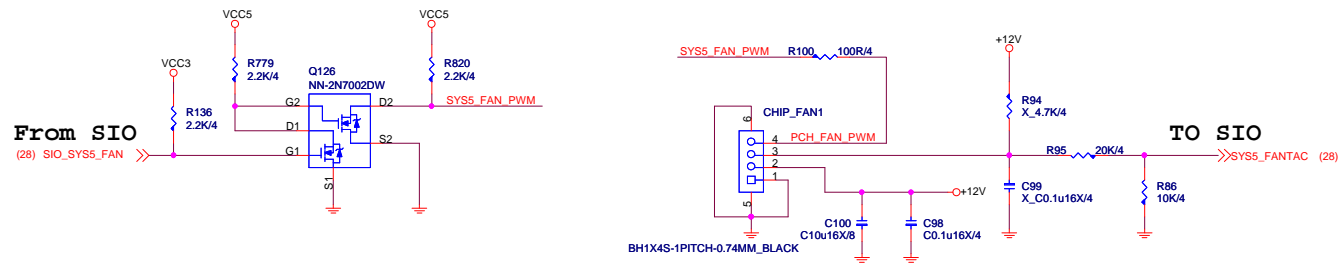


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Size	Document Description	Rev
Custom	FAN TYPE-K SYSFAN3/4	2.1
Date: Friday, April 26, 2019		
Sheet 33 of 75		

# PCH\_FAN



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By PM Define FAN name

SHOW FAN FAULT USE	FAN
GP10	CPUFAN1
GP11	CPUFAN2 PUMPFAN

BIOS SHOW FAN FAULT Information USE  
Default GPI

BIOS SHOW FAN MODE Information USE  
Default GPI

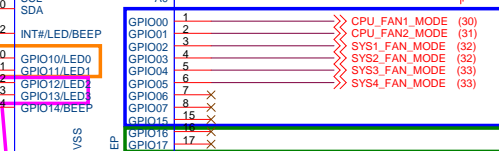
use avoid S5 leakage

CPUFAN1\_FM R47 1K/4

By PM Define FAN name

SHOW FAN MODE USE	FAN
GP12	CPUFAN1
GP13	CPUFAN2 PUMPFAN

slave address :  
Write 4CH  
Read 4DH



By PM Define FAN name

LED OFF BLINK	FAN
GP16	CPUFAN1
GP17	CPUFAN2 PUMPFAN

Default GPI

USE LED OFF & LED BLINK

By PM Define FAN name

FAN MODE USE	FAN
GP00	CPUFAN1
GP01	CPUFAN2 PUMPFAN
GP02	SYSFAN1
GP03	SYSFAN2
GP04	SYSFAN3
GP05	SYSFAN4
GP06	SYSFAN5
GP07	EXT_SYS FAN1
GP15	EXT_SYS FAN2

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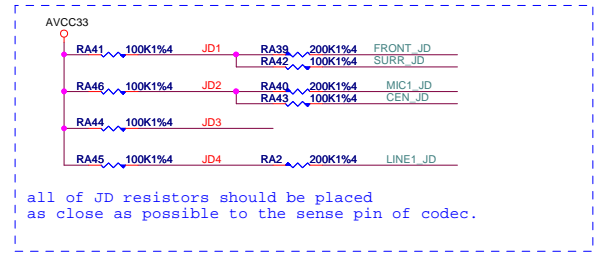
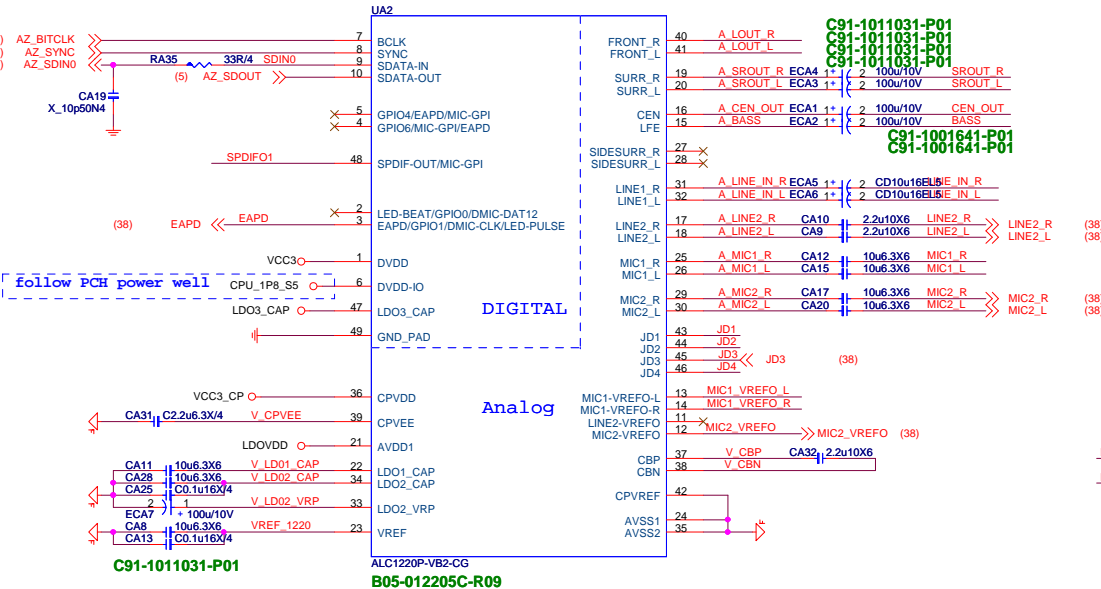
MICRO-STAR INT'L CO.,LTD

MS-7C37

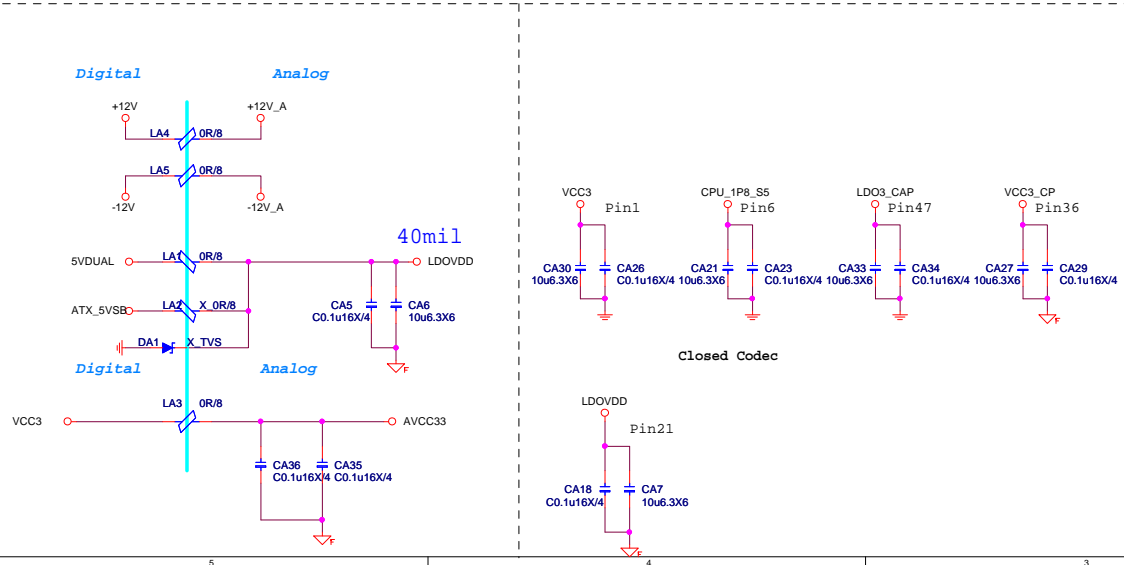
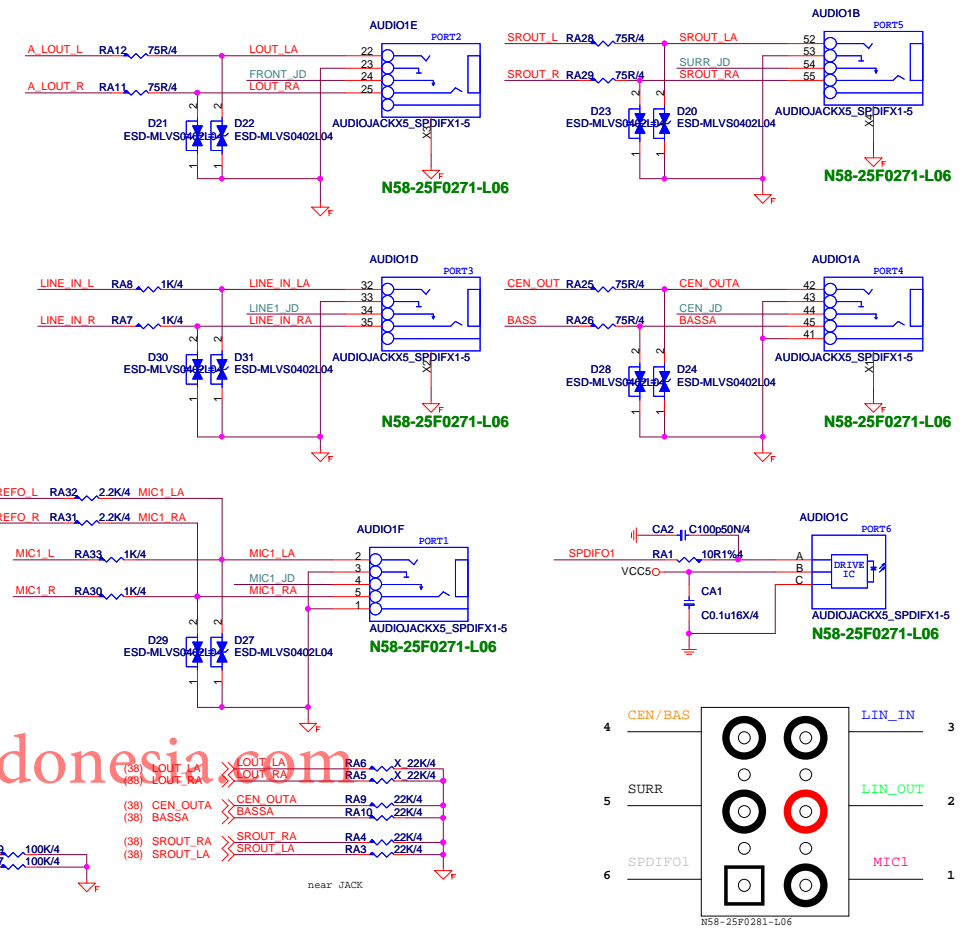
Size Custom	Document Description FAN GPIO NCT5635	Rev 2.1
Date: Friday, April 26, 2019	Sheet 35 of 75	



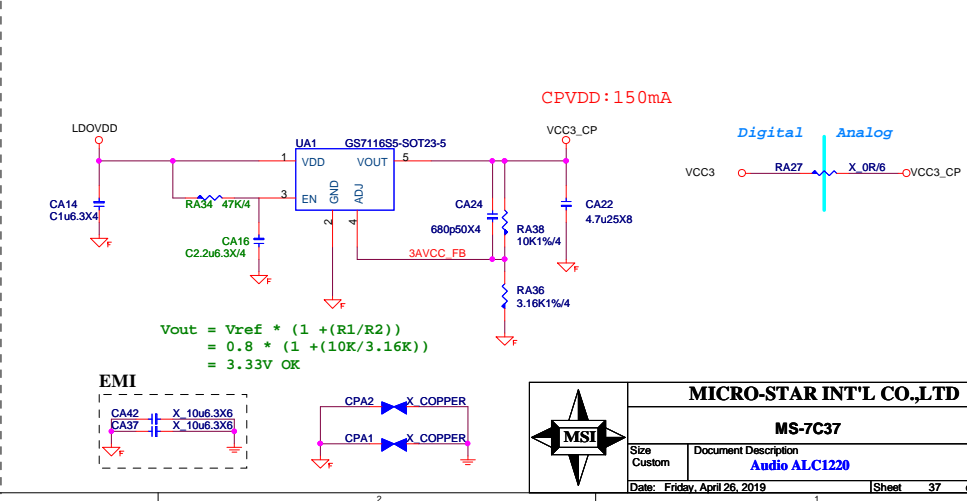
ALC1220P-VB2\_48PIN



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CPVDD POWER: ATX5VSB will Leakage to CVDD by ALC1220, so CVDD must keep 3.3V

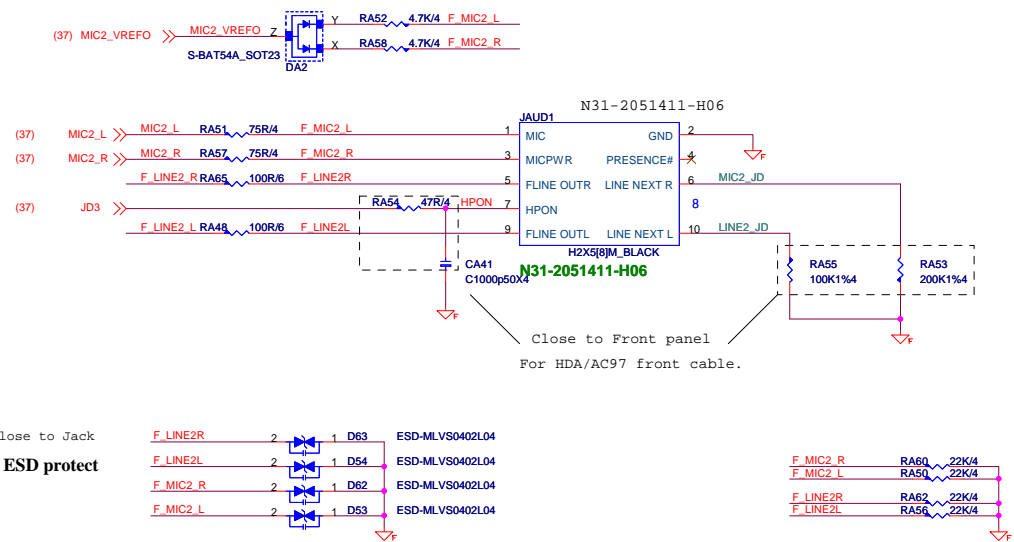
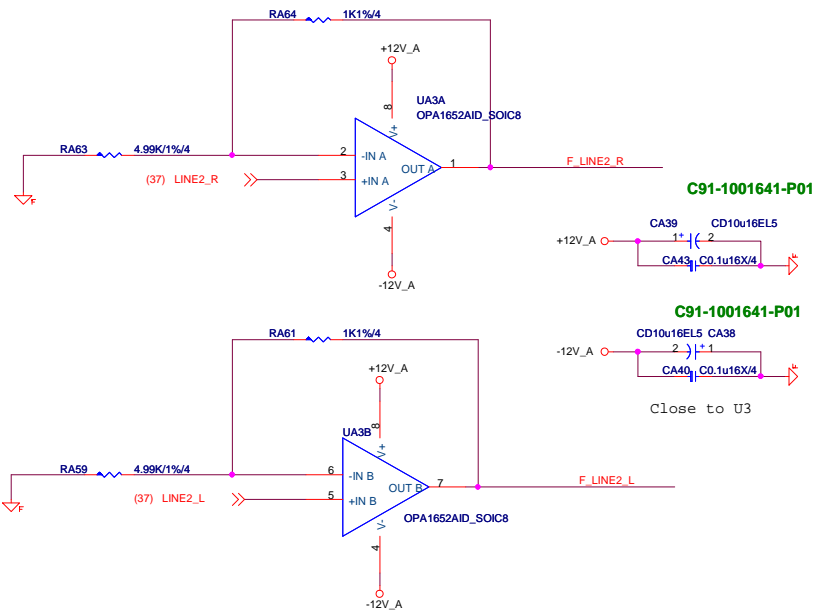


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**MS-7C37**

Size: Custom | Document Description: Audio ALC1220 | Rev: 2.1

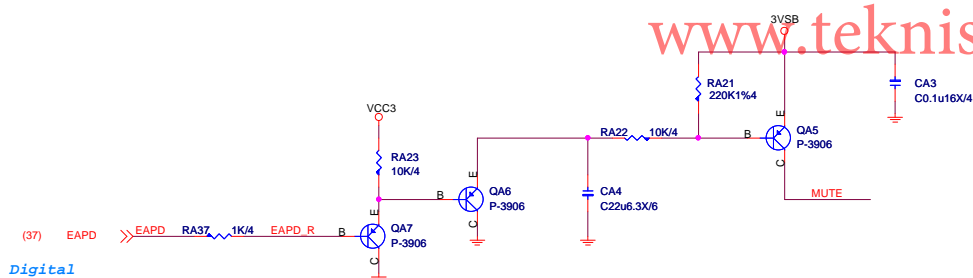
Date: Friday, April 26, 2019 | Sheet: 37 of 75



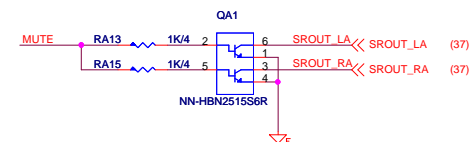
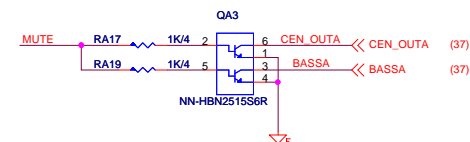
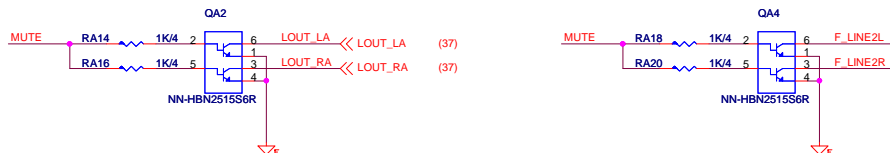
# **Rear Line OUT De-POP circuit** (De-pop circuit for Rear Line out & Front Headphone out)

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(add de-pop circuit by PM spec or customer request,  
NOTE: add de-pop circuit need to change SROUT\_LA, SROUT\_RA, CEN\_OUTA, BASSA to TVS)

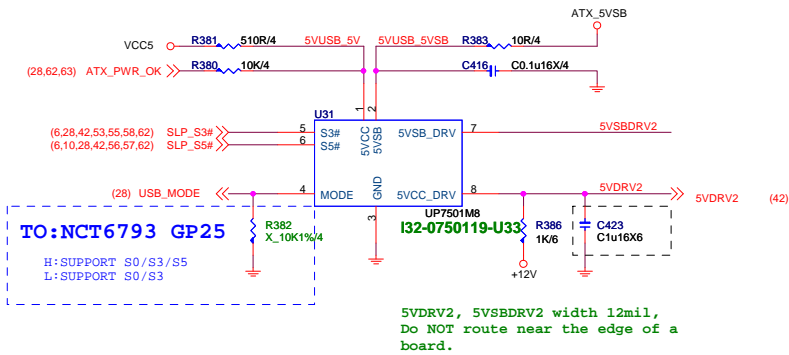


**Analog**

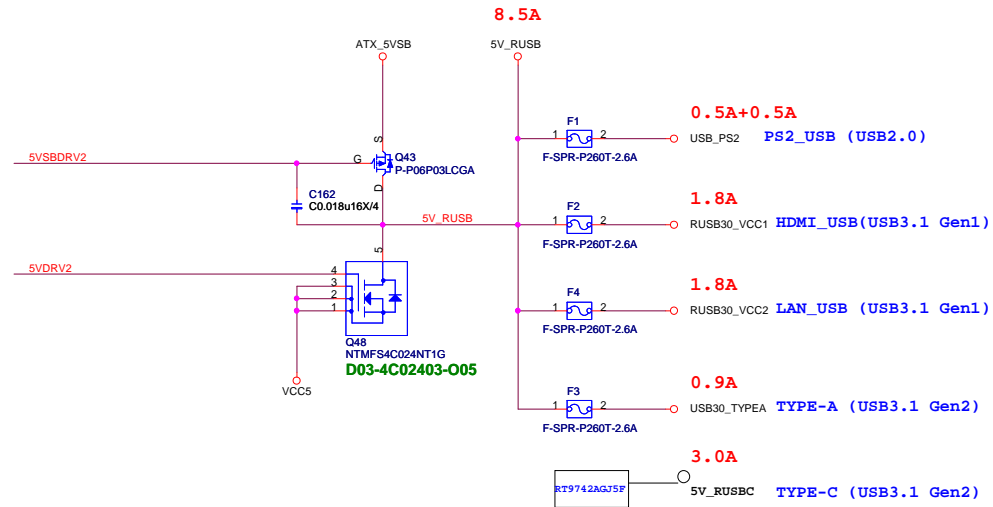


Audio moat is transparent and width 40mil

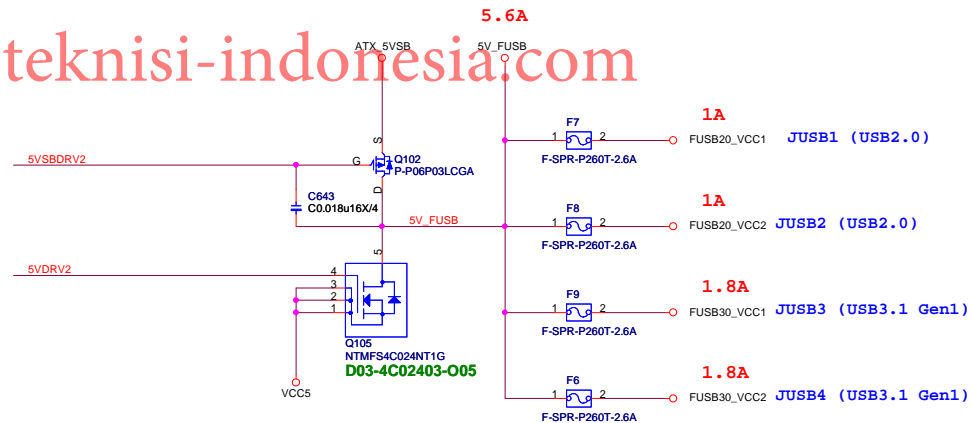
## USB Power



## Rear USB Port Power



## Front USB Port Power



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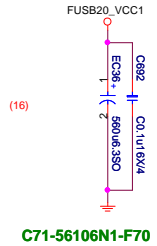
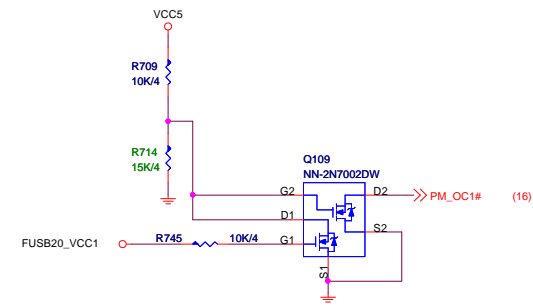
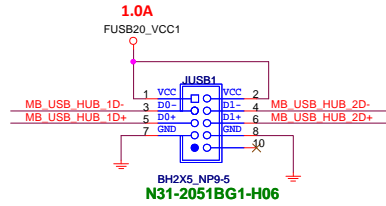
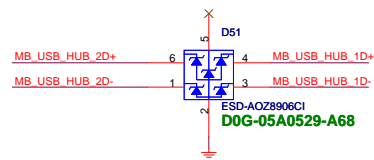
Vinafix.com

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MS-7C37		
Size Custom	Document Description USB Power - UP7501	Rev 2.1
Date: Friday, April 26, 2019	Sheet 39	of 75



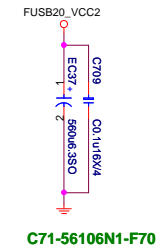
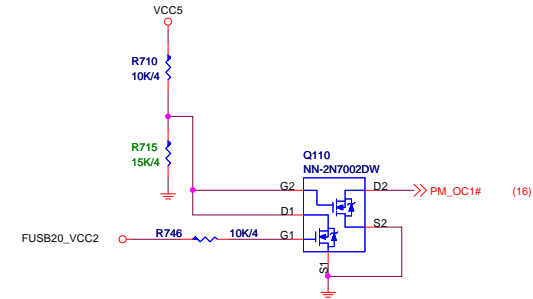
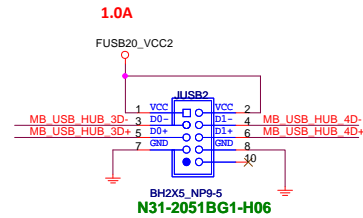
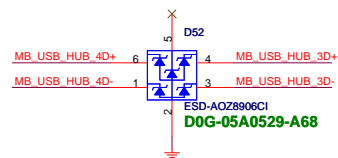
## Front USB2.0(JUSB1)

(46) MB\_USB\_HUB\_1D+ <<>  
 (46) MB\_USB\_HUB\_1D- <<>  
 (46) MB\_USB\_HUB\_2D+ <<>  
 (46) MB\_USB\_HUB\_2D- <<>



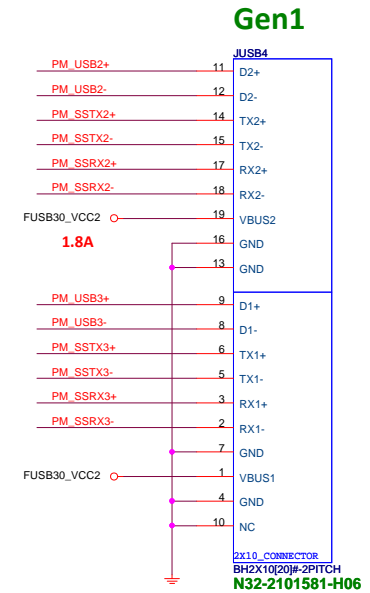
## Front USB2.0(JUSB2)

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 (46) MB\_USB\_HUB\_3D- <<>  
 (46) MB\_USB\_HUB\_4D+ <<>  
 (46) MB\_USB\_HUB\_4D- <<>



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### Front USB3 90° BOX Header(JUSB4)



## PS2

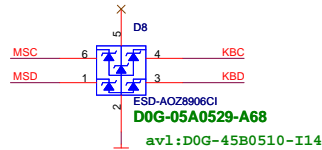
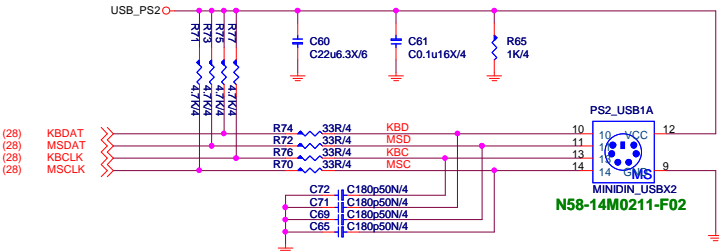
5V@1A

layout note:

C21 must close to TVS pin5

TVS must near KB\_MS1 connector and route without branch

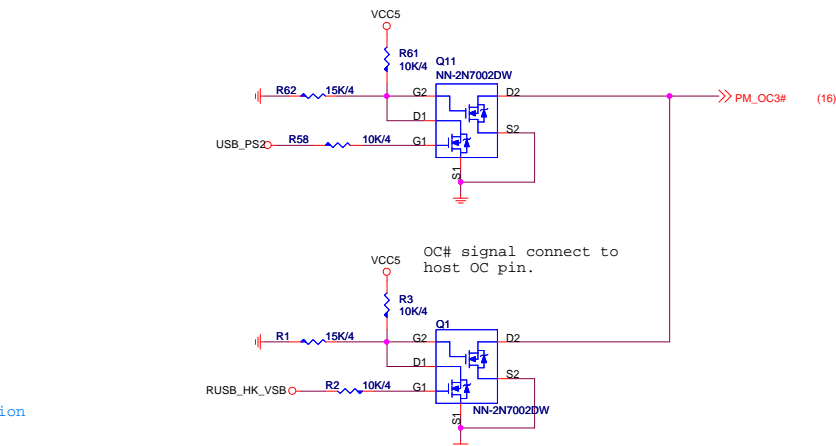
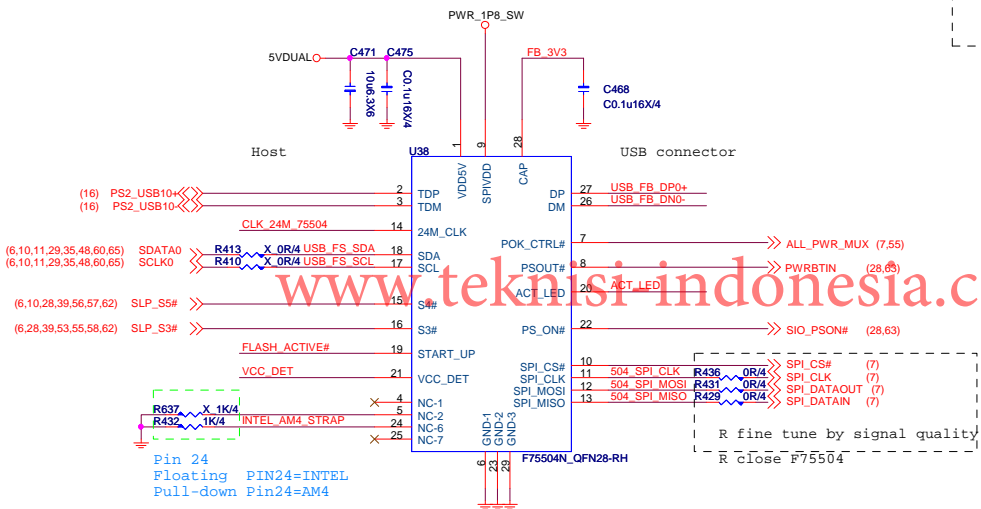
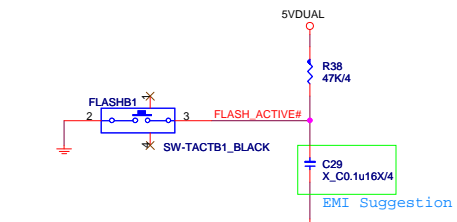
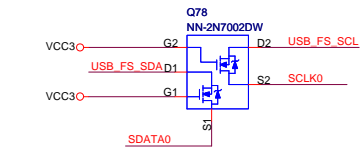
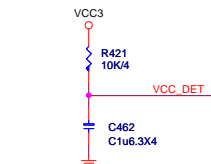
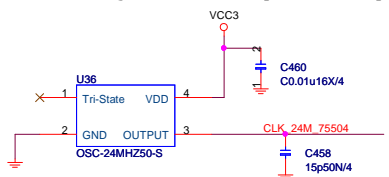
Varistor must close to TVS and route without branch



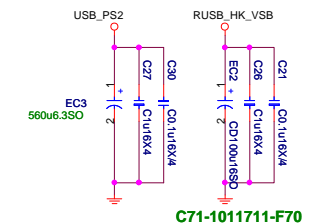
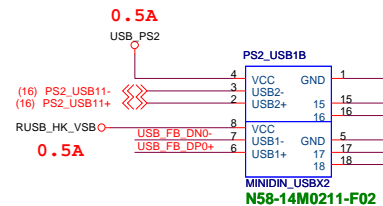
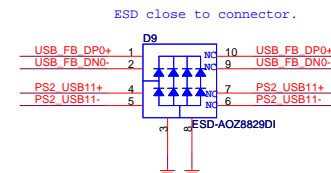
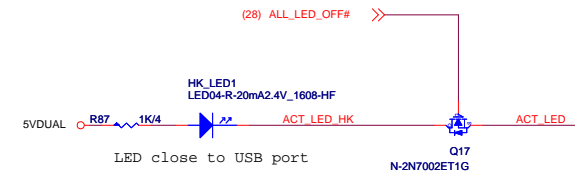
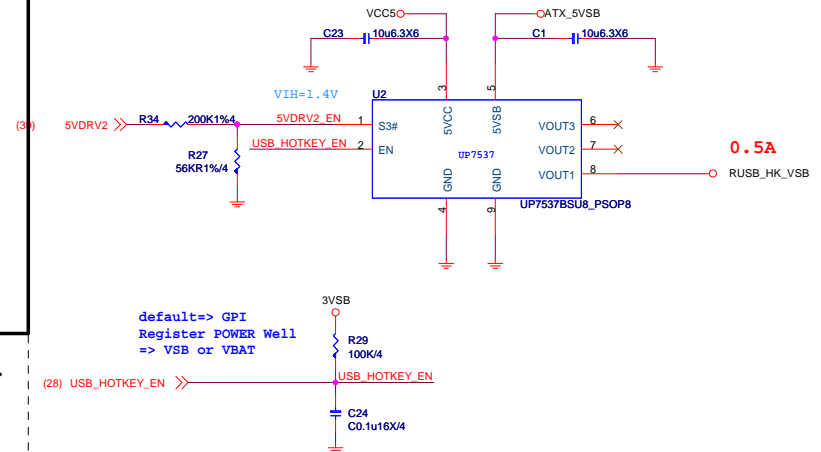
## USB2.0 Flash BIOS

F75504 layout placement must meet to spi/usb trace length spec with host.  
As for as possible place near to host.

CLK running in S0,don't require in sleep



## HOTKEY POWER



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Size Custom Document Description Rear USB2.0 + PS2 Rev 2.1  
Date: Friday, April 26, 2019 Sheet 42 of 75

## 0.13A

1~5"



## 1.8A



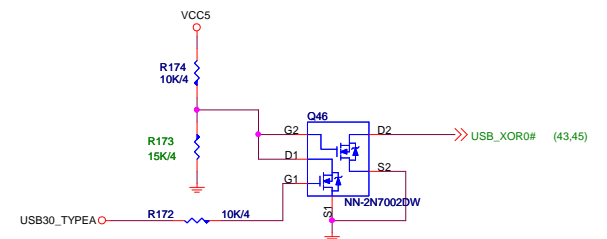
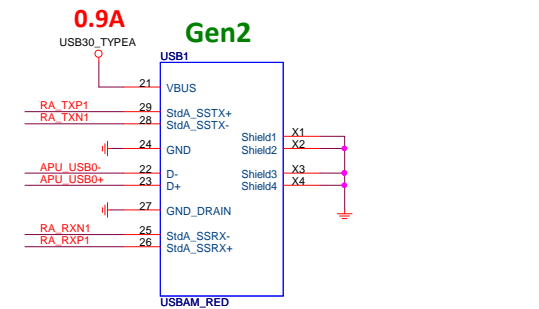
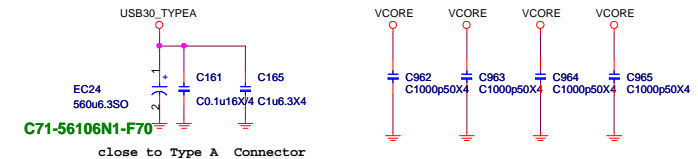
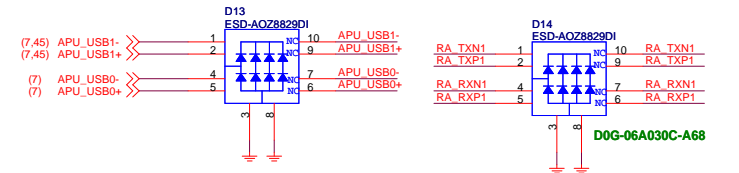
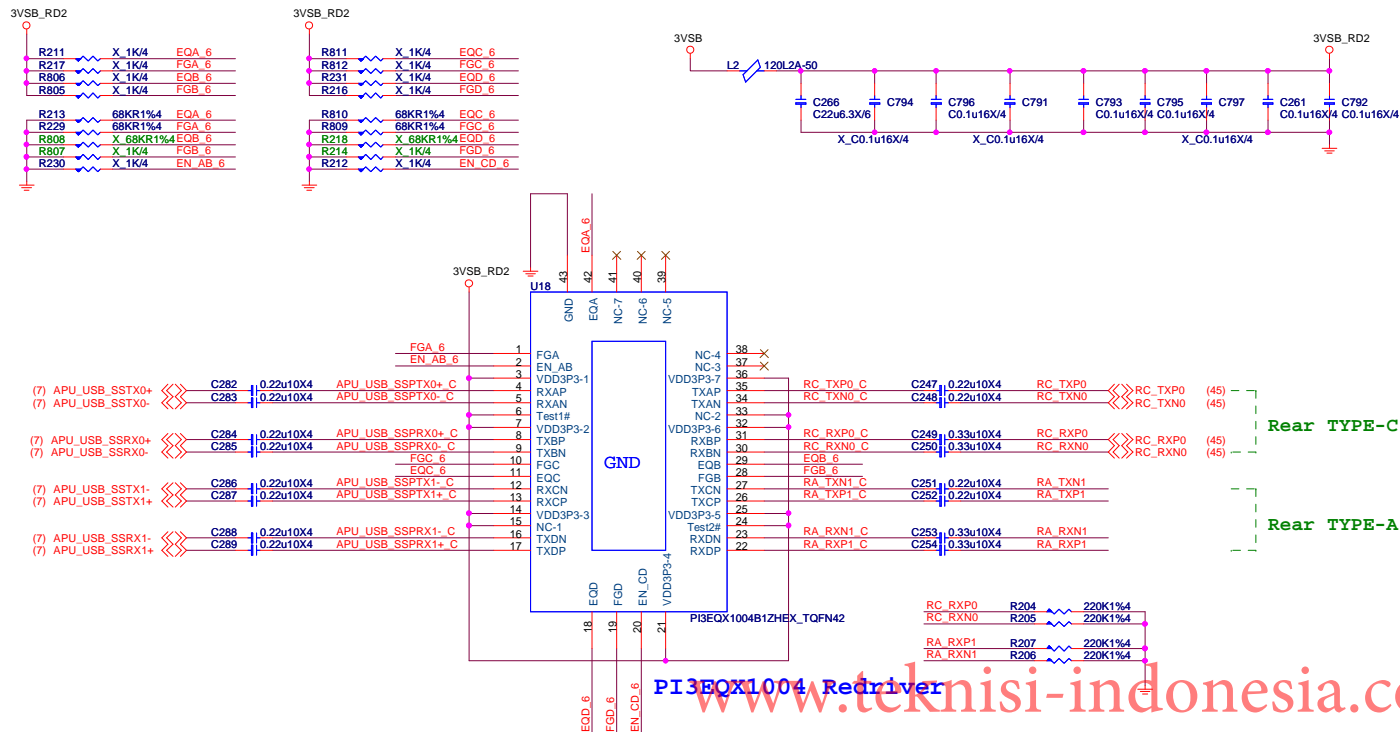
## Type1/2/3/4 High Active



MS-7C37

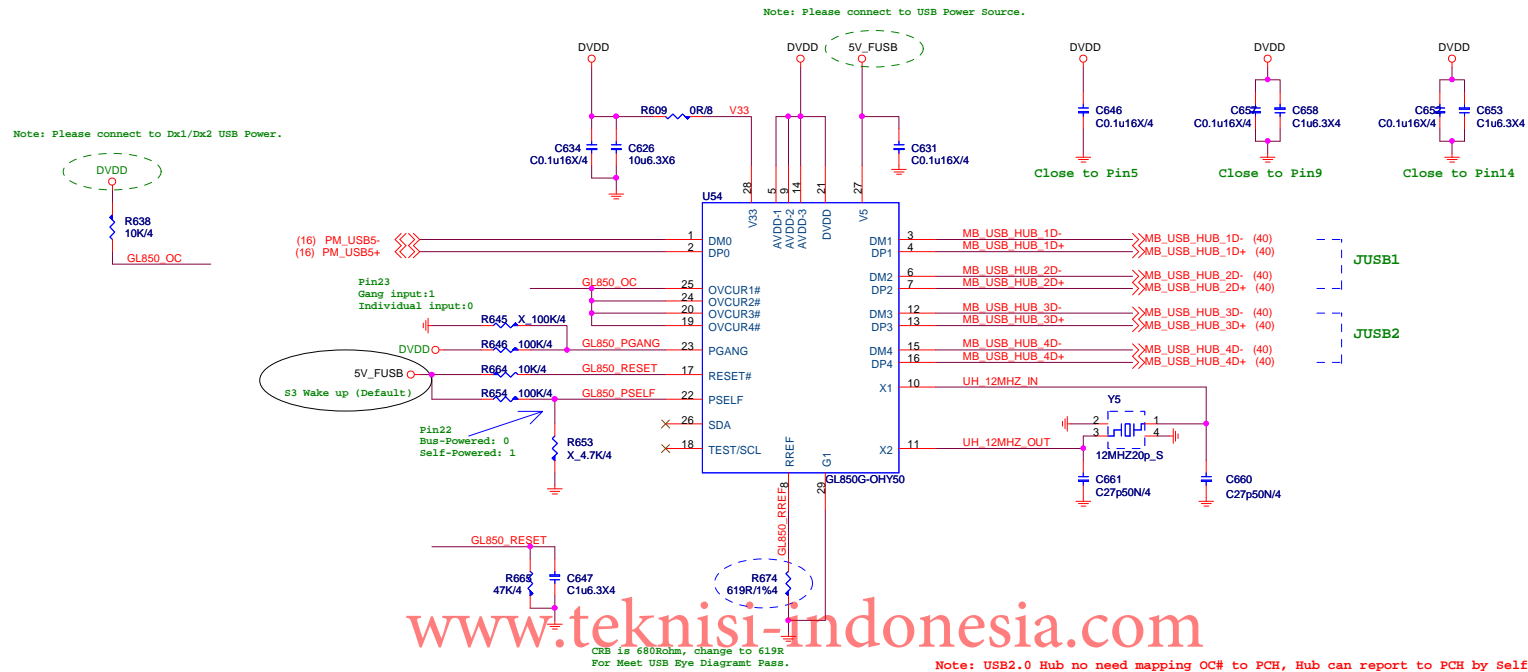
Size Custom	Document Description <b>Rear_USB3.0 * 4</b>	Rev 2.1
Date: Friday, April 26, 2019		Sheet 43 of 75

# USB3.1 Gen2 Redriver + Type-A





## 5V\_FUSB



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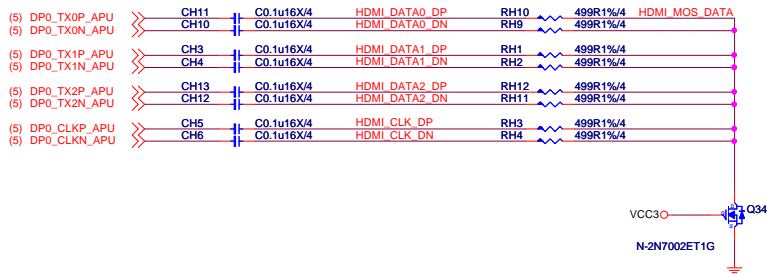
MS-7C37

Size Custom	Document Description <b>GL850G</b>	Rev 2.1
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# HDMI CONNECTOR

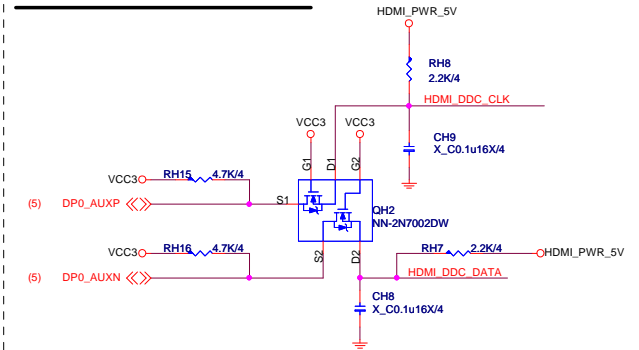
For HDMI 1.4



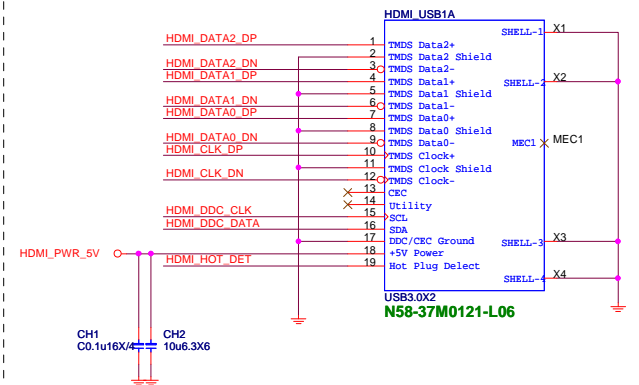
刪除RH6/RH12/RH15/RH16  
For 增加VCC5寬度

For EMI

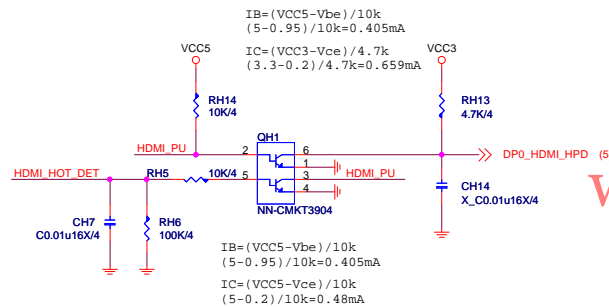
## AUX Level Shifter



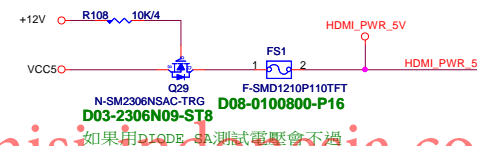
## Connector



## HPD Circuit

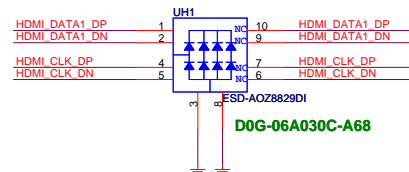
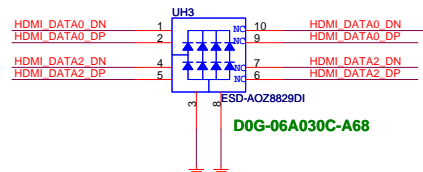


## Connector Power

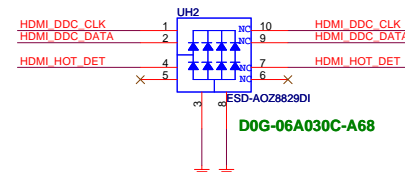


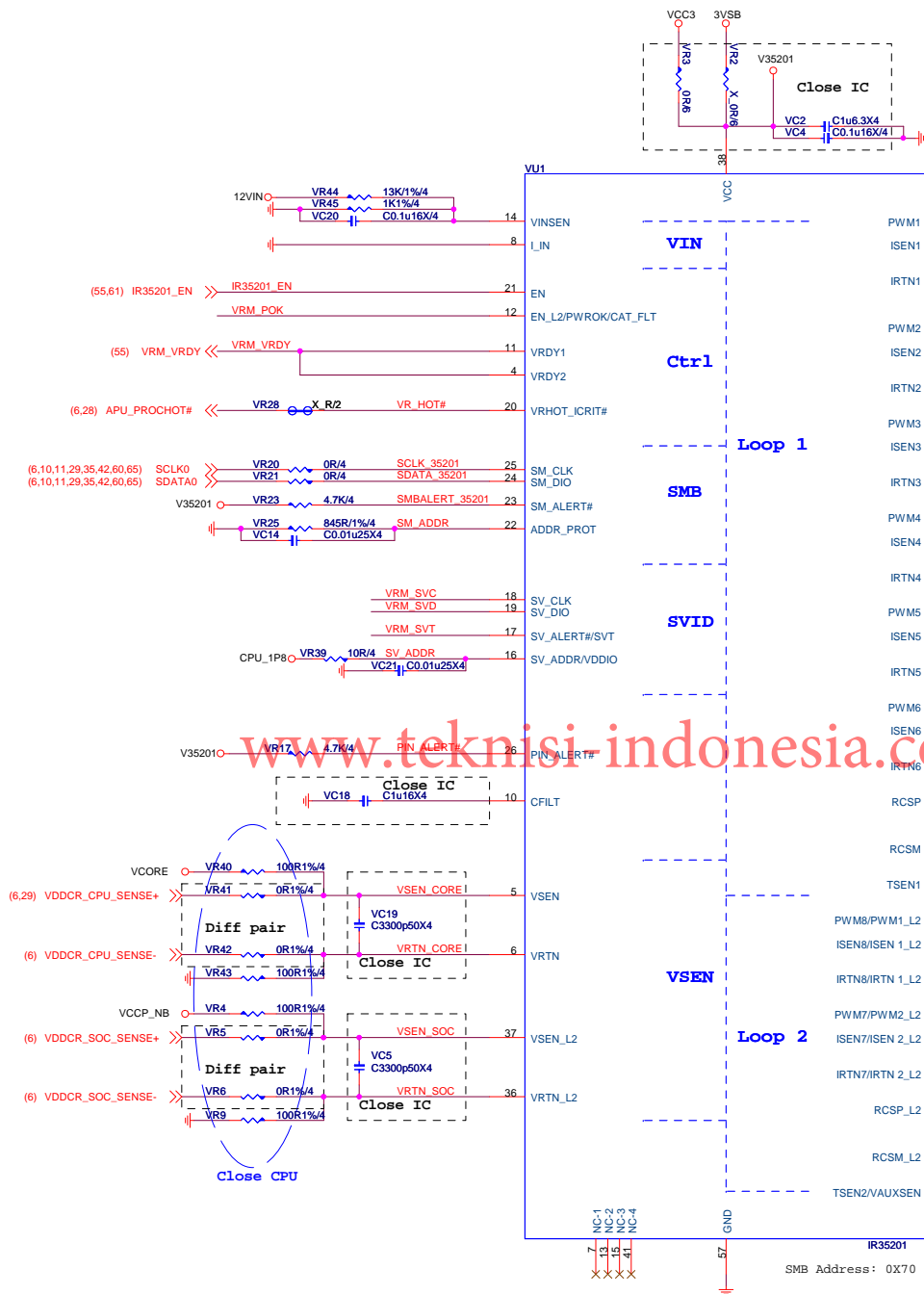
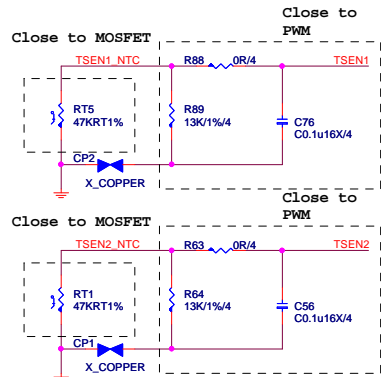
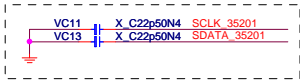
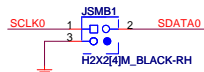
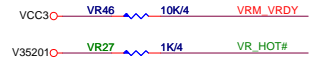
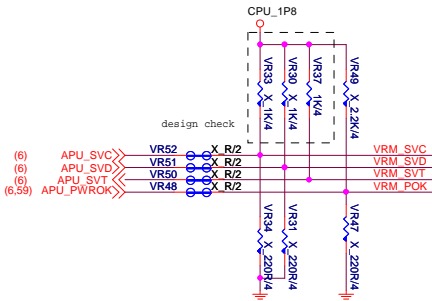
如果用DIODE SA測試電壓會不過

## For EMI



## 注意:耐壓5V零件



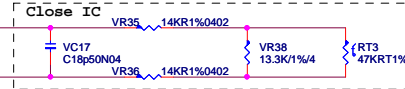


燒錄打點:IC正面上橋+金色點

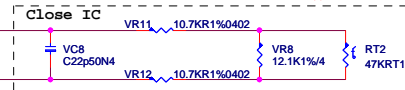
VCORE: ICCMax 140A  
LL: 1.3mohm  
OCP: 192A  
SOC: ICCMax 75A  
LL: 2.1ohm  
OCP: 90A

Phase 1 close to CPU power pin.

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RT close to Choke



RT close to Choke

0x26:RH=18K,RL=13K							
Default	VR53	VR54	VC20	VR58	VR57	VR59	VR60
Temp	6.49k	10k	100p	X	0R	X	0R
VAUXSEN	5.76k	1k	0.01u	0R	X	0R	X

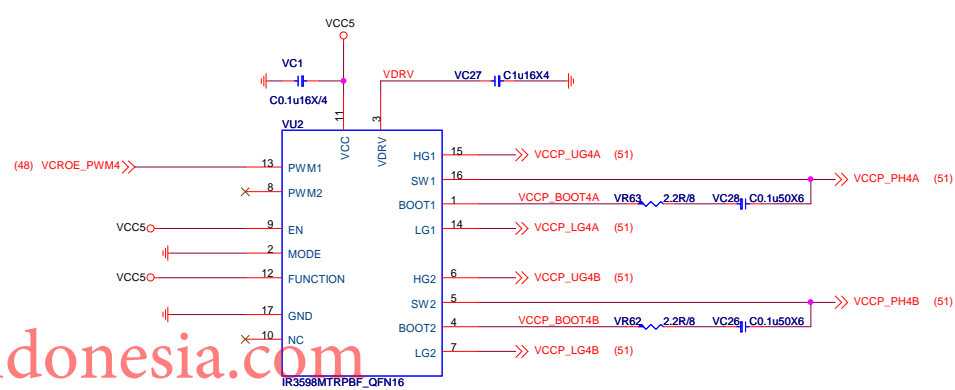
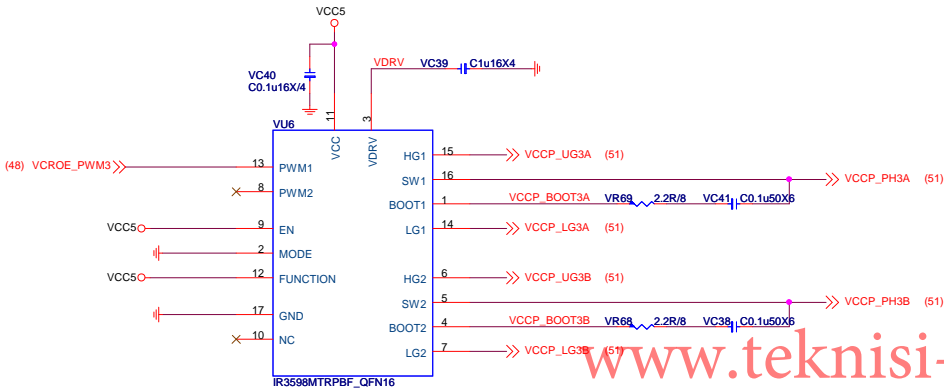
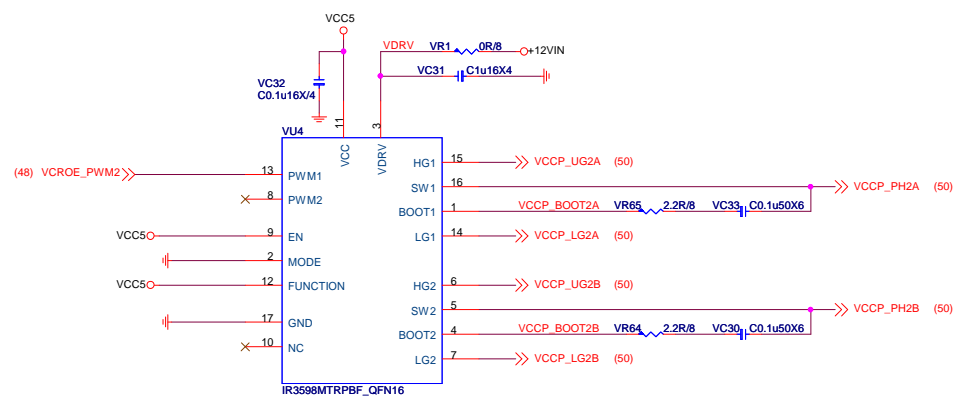
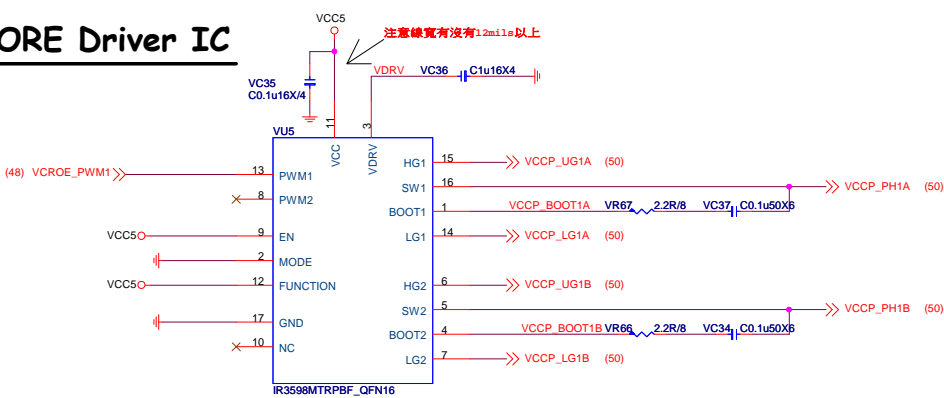


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Custom	CPU Power IR35201 8+2	2.1
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CPU\_CORE Driver IC



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CPU\_SOC Driver IC

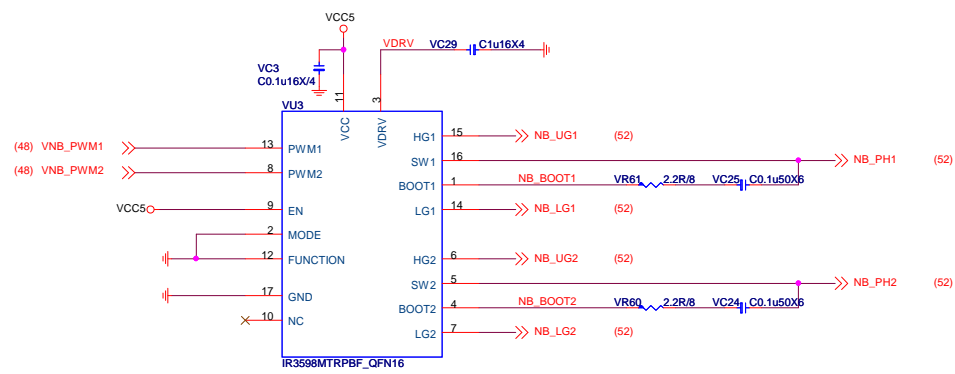


Table for IR3598

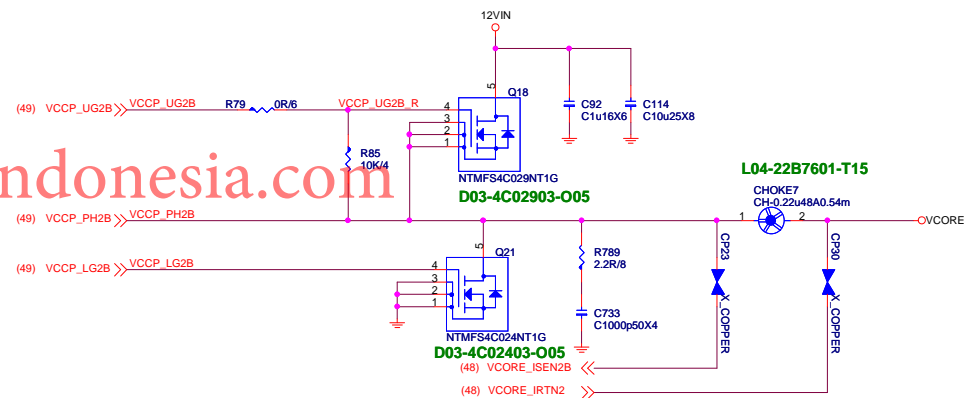
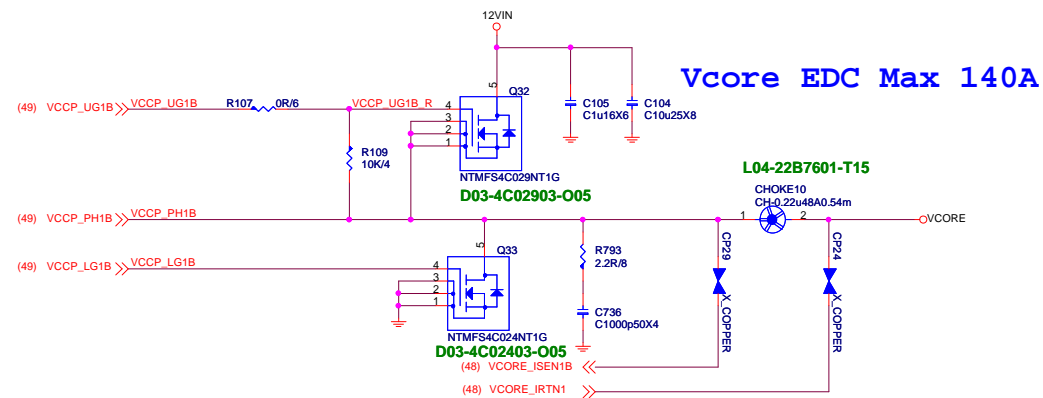
Function	Mode	PWM Mode	Phase Mode	
0	1	IR ATL	Dual	
1	1	IR ATL	Doubler	
0	0	Tri-State	Dual	SOC
1	0	Tri-State	Doubler	Vcore

**MICRO-STAR INT'L CO.,LTD**

**MS-7C37**

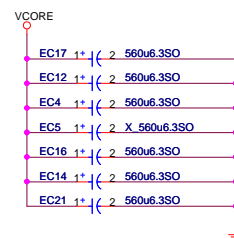
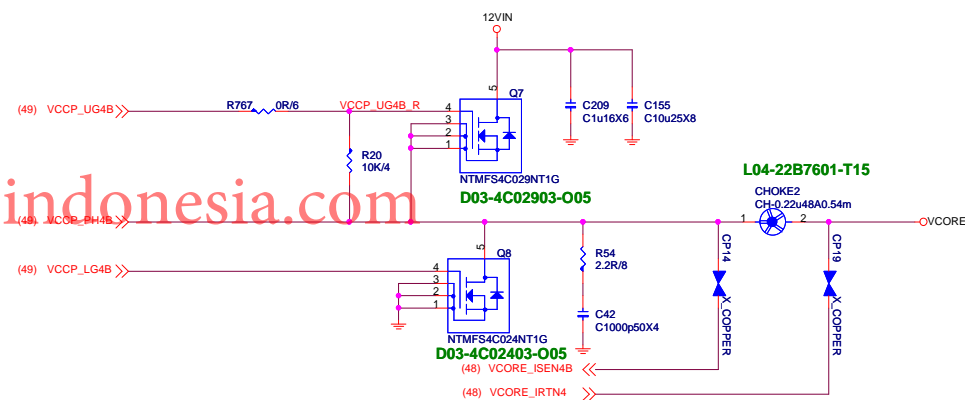
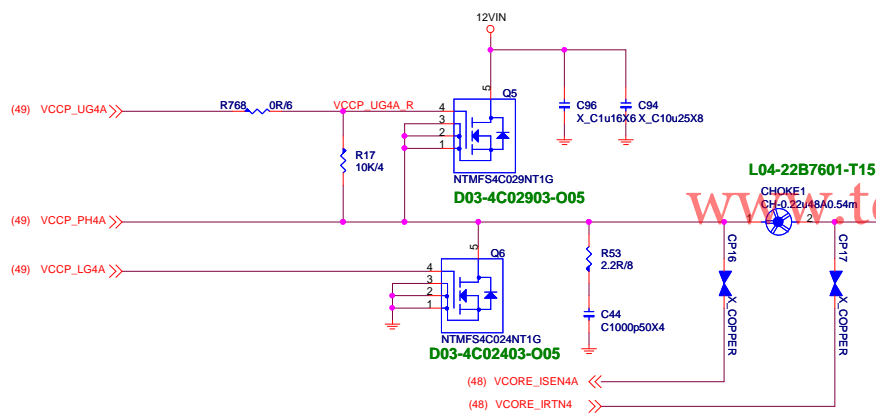
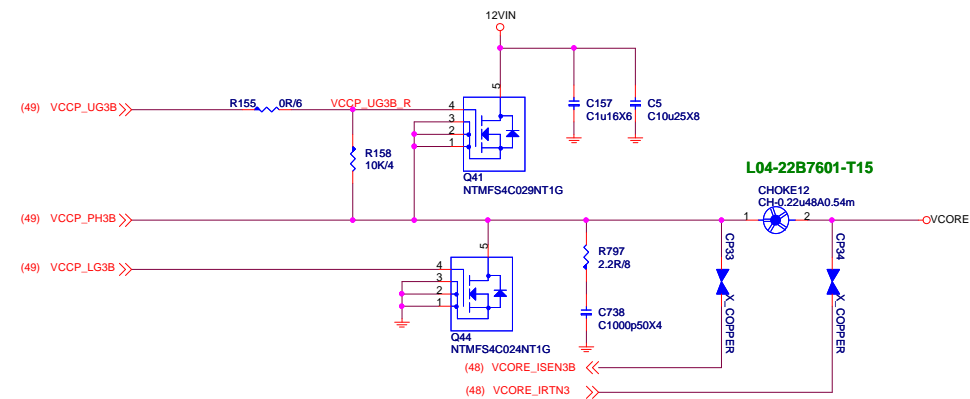
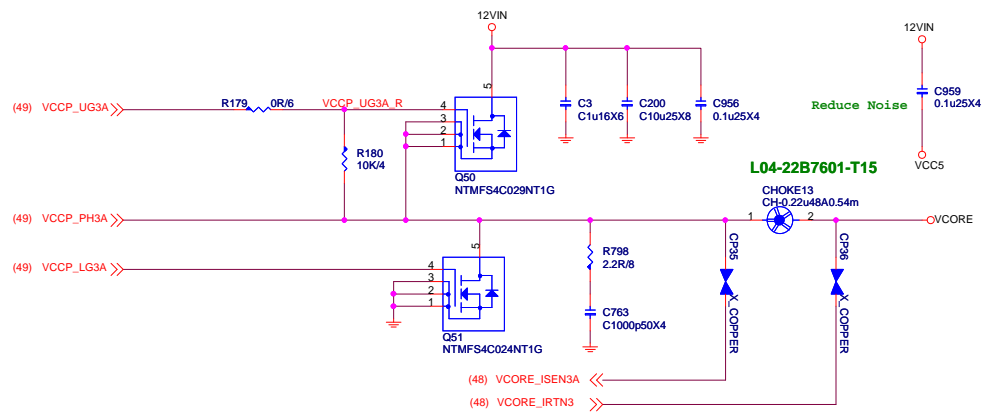
Size Custom Document Description **CPU Power Driver IC IR3598** Rev 2.1

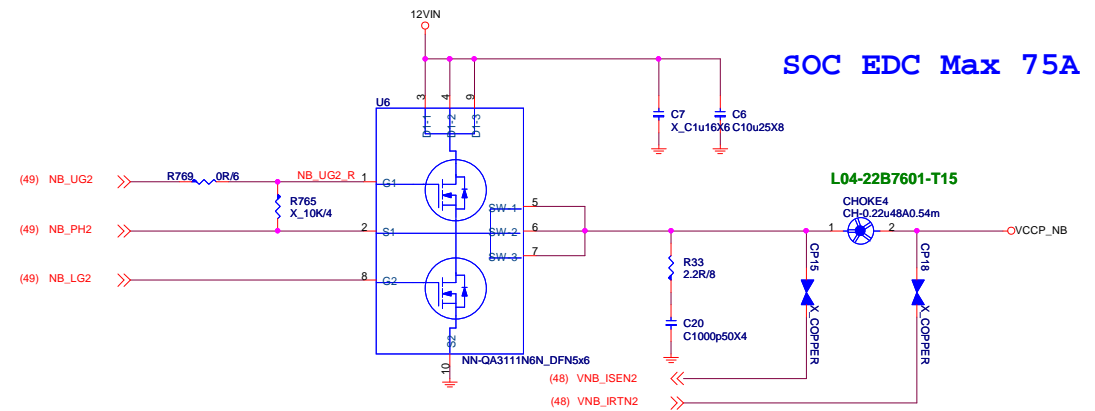
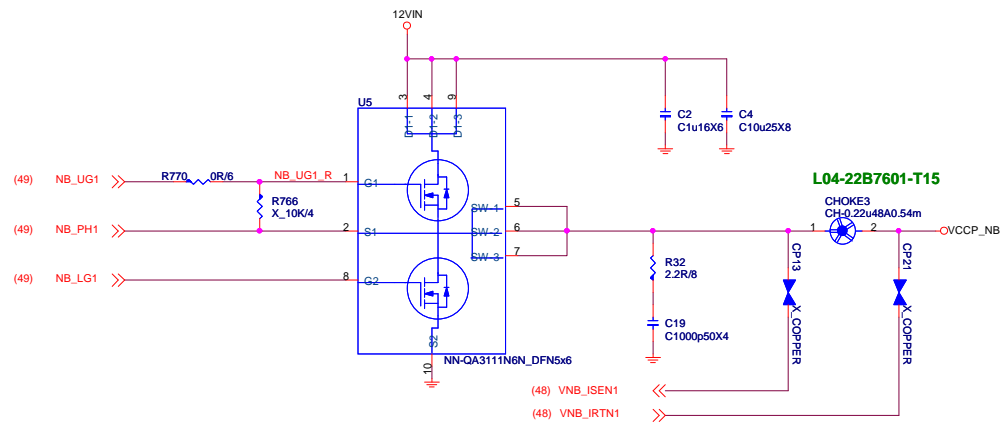
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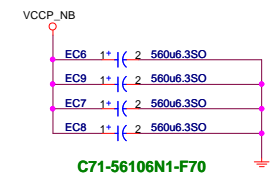
Size Custom	Document Description <b>CPU Power Vocre Phase 1-6</b>	Rev 2.
Date: Friday, April 26, 2019		Sheet 50 of 75





SOC EDC Max 75A

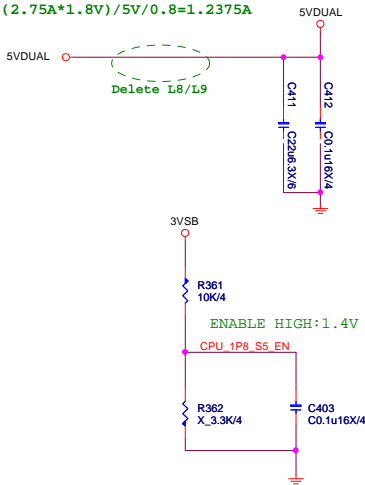
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```
CPU: VDD_18_S5@0.5A
CPU: VDDIO_Audio@0.25A
CHIP: VDD_18_S5@0.1A
```

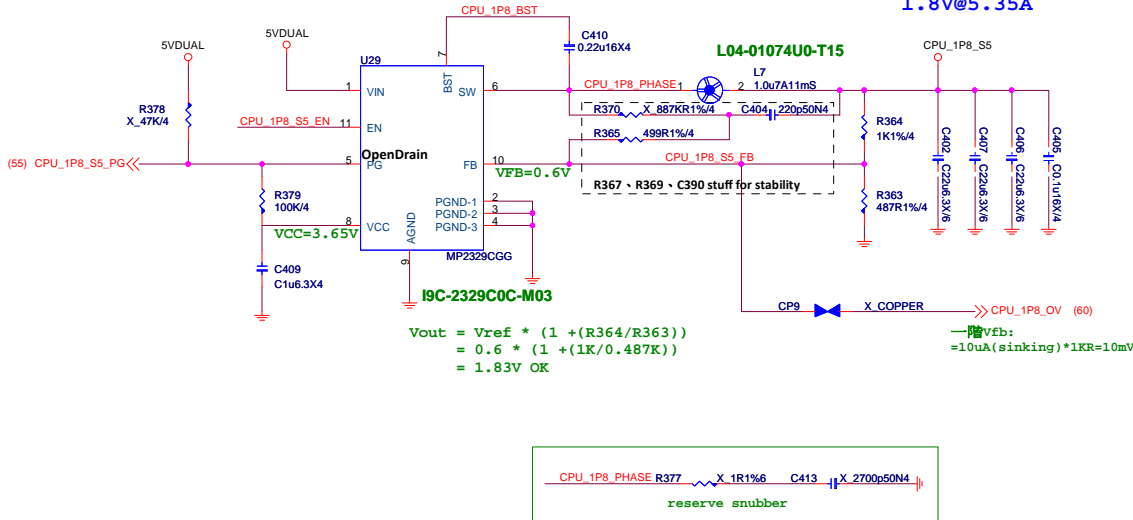
```
CPU_1P8: 2.5A
CPU_VDDP_S5: 1A
CHIP_SOC_S5: 1A
```

Input Current=  
 $(2.75\text{A} \cdot 1.8\text{V}) / 5\text{V} / 0.8 = 1.2375\text{A}$



CPU\_1P8\_BST、CPU\_1P8\_BST\_R >50 mils.

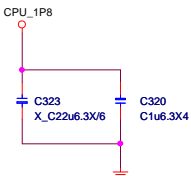
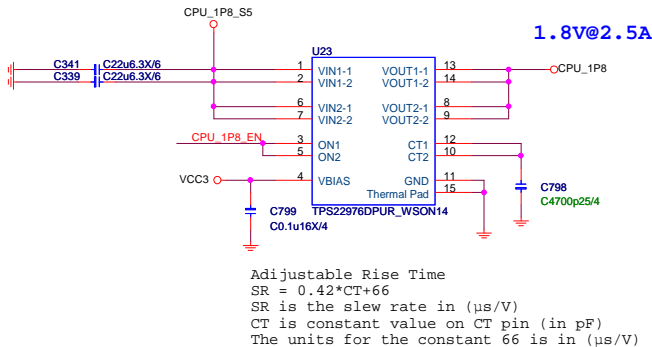
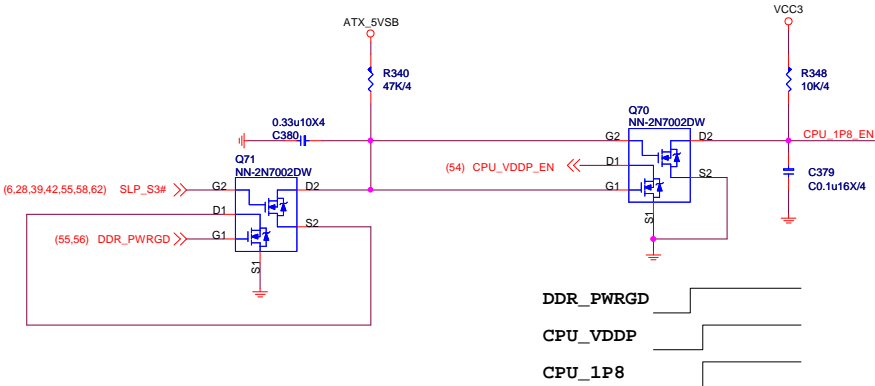
1.8V@5.35A



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CPU: VDD\_18@2A  
CHIP: VDD\_18@0.5A

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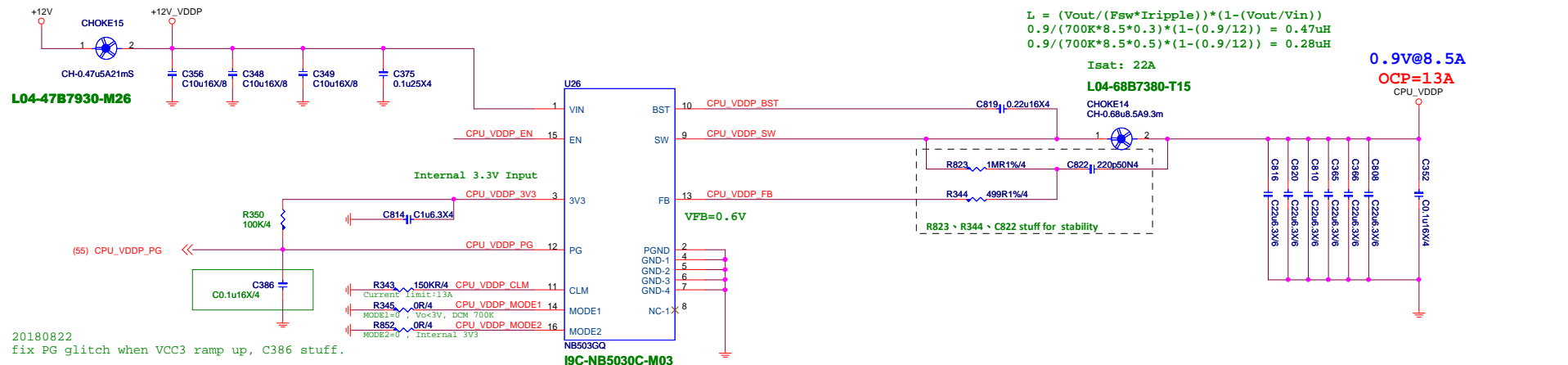


<b>MICRO-STAR INT'L CO.,LTD</b>			
<b>MS-7C37</b>			
Size Custom	Document Description <b>CPU Power 1.8_S0/S5</b>		Rev 2.1
Date: Friday, April 26, 2019		Sheet 53 of 75	

## CPU\_VDDP

CPU: VDDP@8.5A

Input Current =  $(8.5A \cdot 0.9V) / 12V / 0.8 = 0.8A$   
 Choke Isat = 8A  
 $I_{rms} = I_{out} \cdot \sqrt{((V_o/V_i) \cdot (1 - (V_o/V_i)))}$   
 $= 13 \cdot \sqrt{((0.9/12) \cdot (1 - (0.9/12)))} = 3.42A$   
 Choke I<sub>rms</sub> = 5A



No support BR SPEC

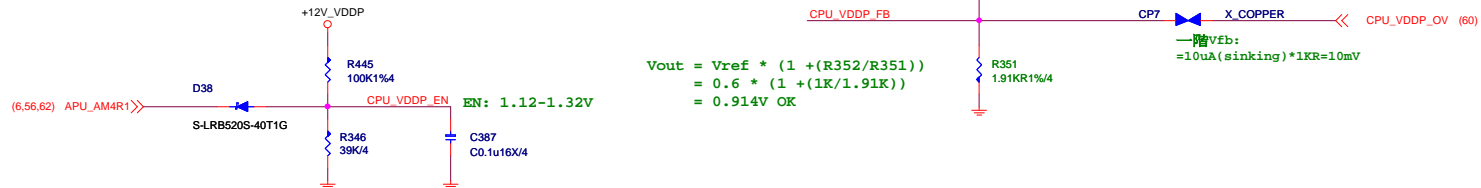
TYPE0\_CPU\_SEL  
 0:RV  
 1:BR/SR/PR/MTS

CPU\_VDDP\_EN:  
 X: BR/SR/PR/MTS  
 0: RV

(6,7,55) TYPE0\_CPU\_SEL >>> CPU\_VDDP\_EN (53)

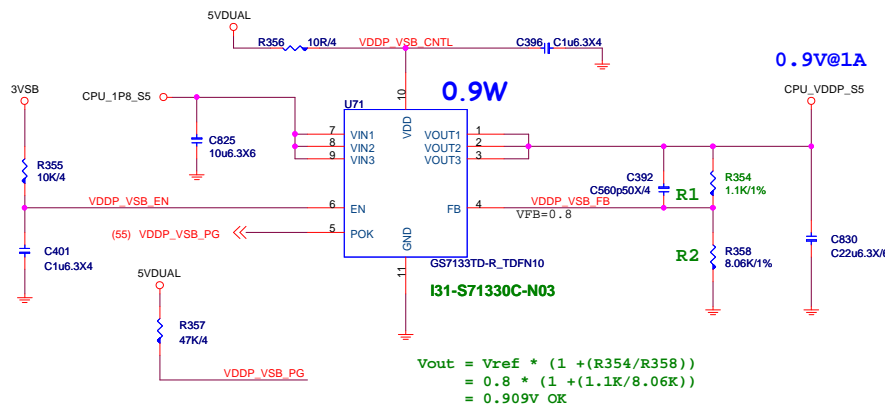
CPU	TYPE	TYPE0_CPU_SEL	CPU_VDDP_EN
BR	0	1	0
NA	1	0	0
SR	2	1	1
RV/ZP	3	0	1
MTS	4	1	1

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## CPU\_VDDP\_S5

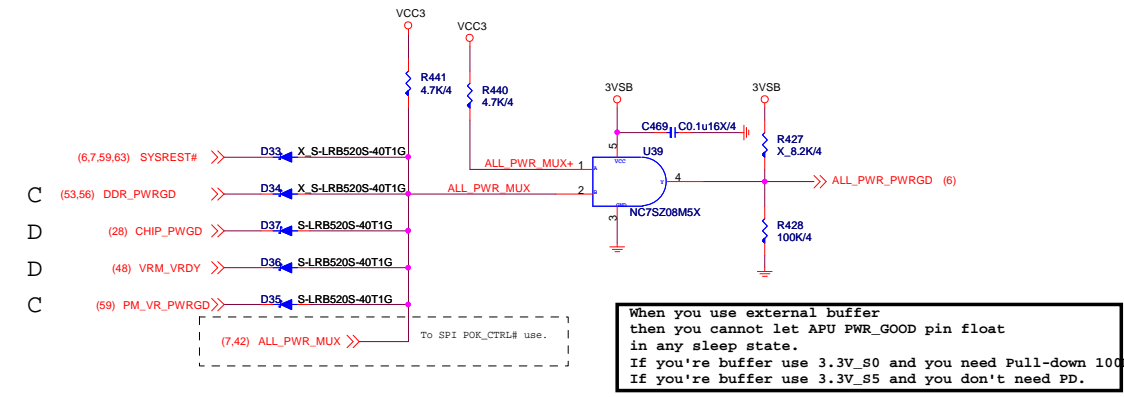
CPU: VDDP\_S5@1A



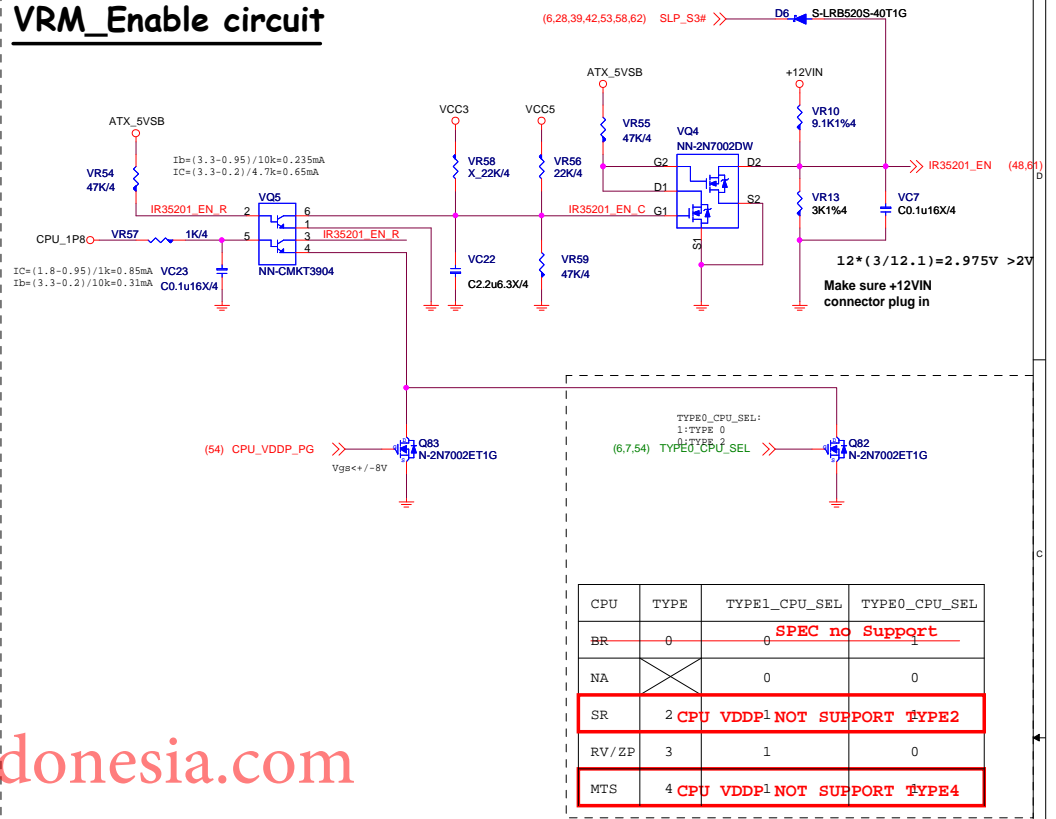


ALL POWER GOOD MUX

S0 PG

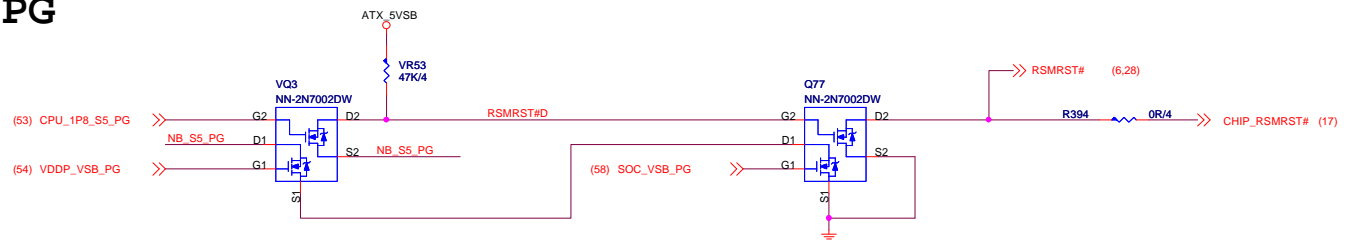


VRM\_Enable circuit



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S5 PG



15.5A For CPU  
9.5A For 4DIMM  
1.2A For DDR VTT

$$R_{OCSET} = \frac{I_{VALLEY} \times R_{LGDS(ON)}}{I_{OCSET}}$$

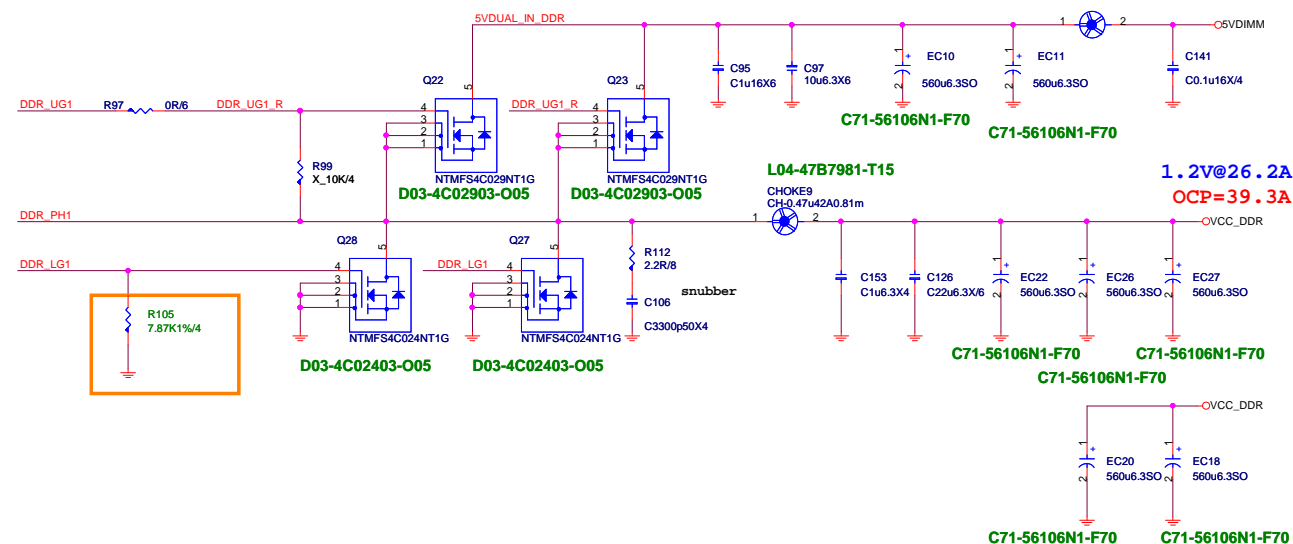
Current Sensing				
ioset			9	10



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Input Current =  $(26.2 \times 1.2) / 5 / 0.8 = 7.86 \text{ A}$

**L04-12A7811-T15**

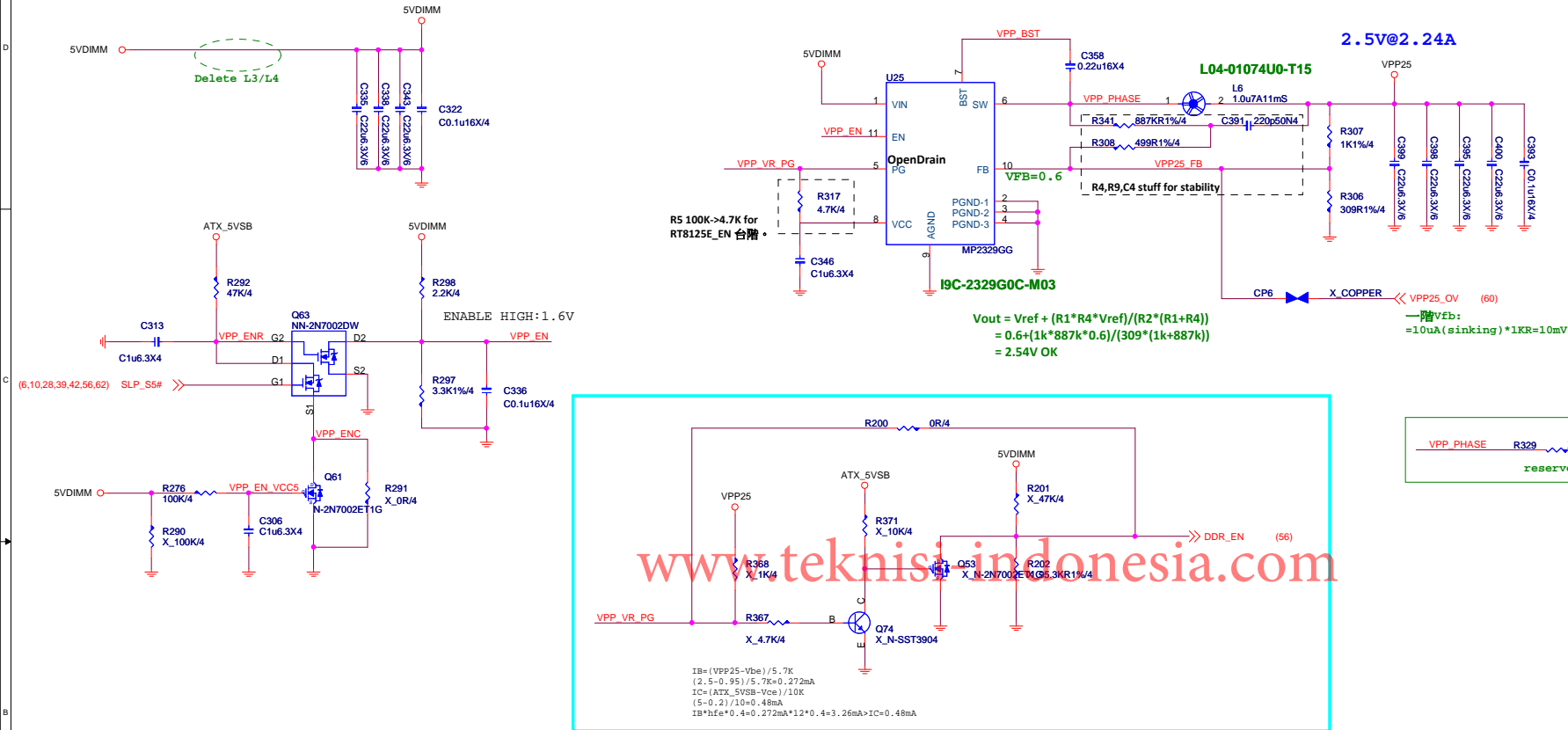


MS-7C37

Size Custom	Document Description <b>DDR Power - 8125E</b>	Rev 2.
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## VPP25

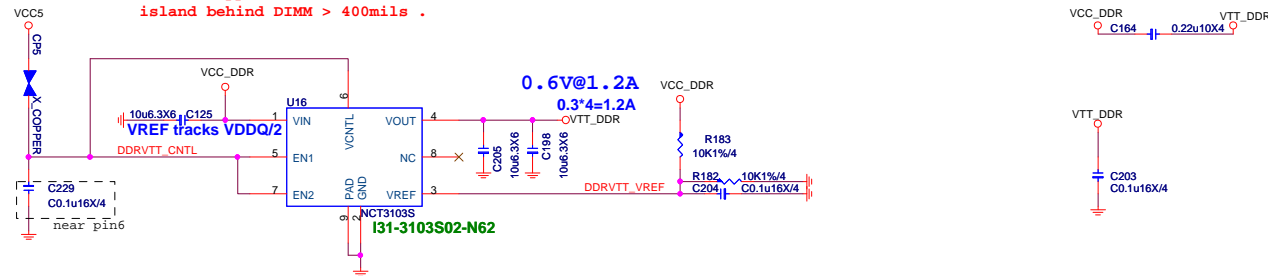
2.5V@2.24A



## VTT\_DDR

0.6V@1.2A

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



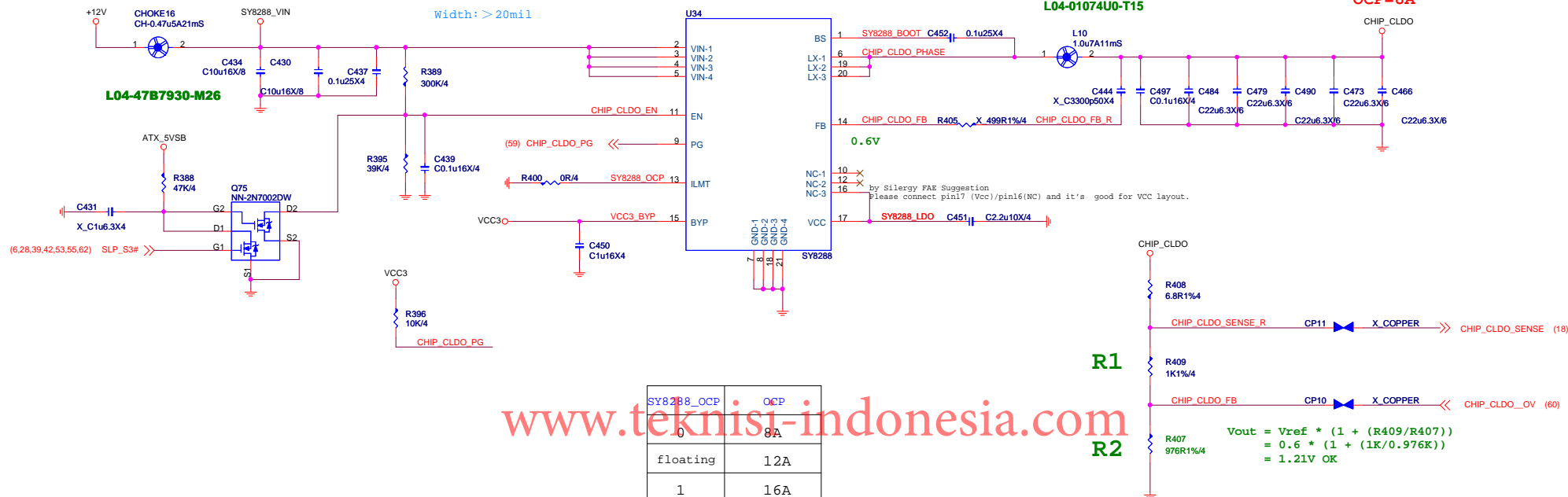
MICRO-STAR INT'L CO.,LTD		
MS-7C37		
Size	Document Description	Rev
Custom	DDR VPP25 / VTT	2.1
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## CHIP\_CLDO

CHIP: VDD\_CLDO@5A

Input Current= (5.5A\*1.05V)/12V/0.8=0.625A

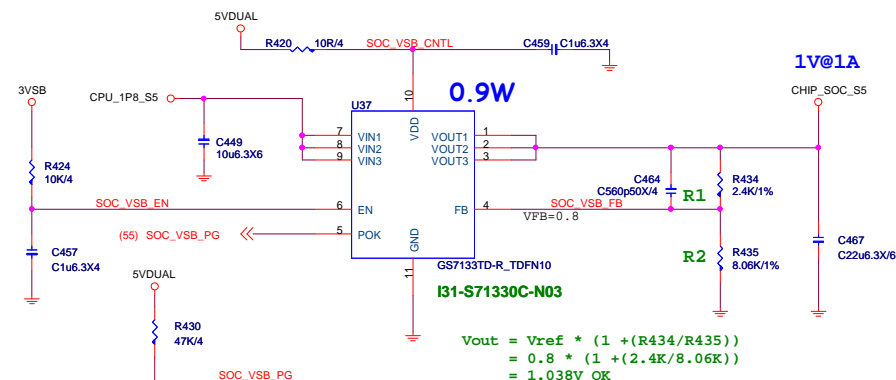
1.2V@5A  
OCP=8A



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## CHIP\_SOC\_S5

CHIP: VDDCR\_SOC\_S5@1A



MICRO-STAR INT'L CO.,LTD

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Custom	PROM - SY8288RAC / 1.05V	2.1
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# CHIP\_SOC

CHIP: VDDCR\_SOC@9A

Input Current =  $(12A \cdot 1V) / 12V / 0.8 = 1.25A$   
 Choke Isat = 8A  
 $I_{rms} = I_{out} \cdot \sqrt{((V_o/V_i) \cdot (1 - (V_o/V_i)))}$   
 $= 12 \cdot \sqrt{((1/12) \cdot (1 - (1/12)))} = 3.316A$   
 Choke  $I_{rms} = 5A$

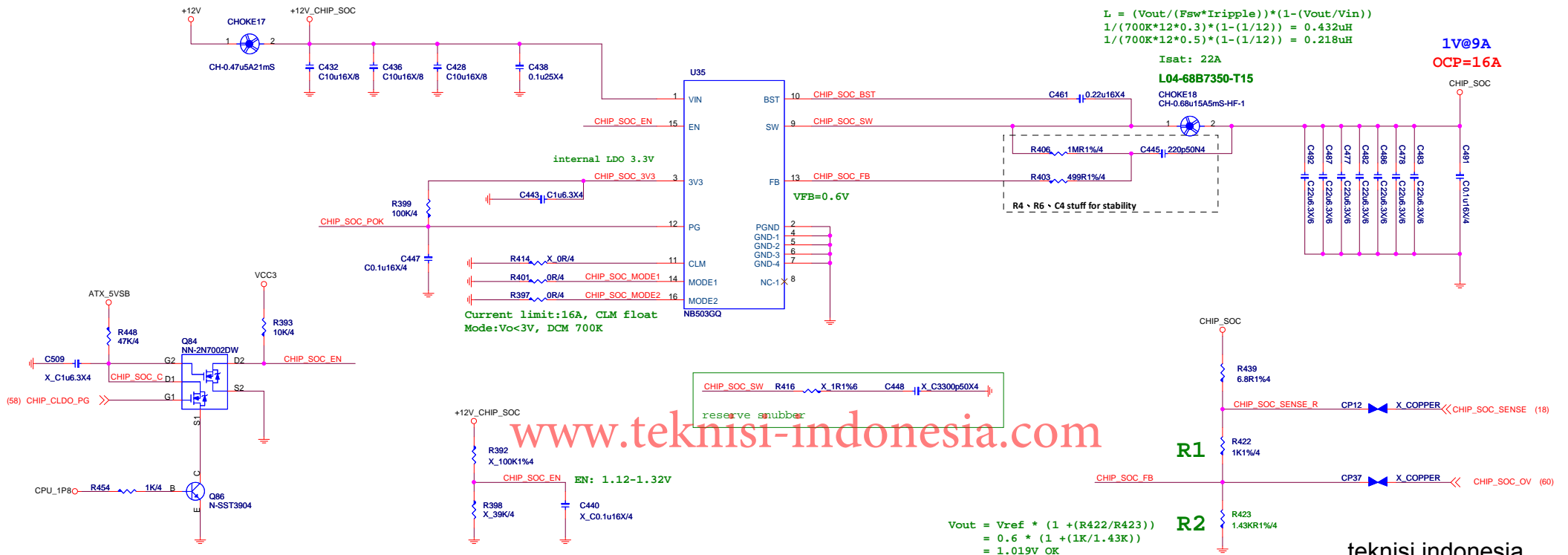
$L = (V_{out} / (F_{sw} \cdot \Delta I_{ripple})) \cdot (1 - (V_{out}/V_{in}))$   
 $1 / ((700K \cdot 12 \cdot 0.3) \cdot (1 - (1/12))) = 0.432uH$   
 $1 / ((700K \cdot 12 \cdot 0.5) \cdot (1 - (1/12))) = 0.218uH$

Isat: 22A

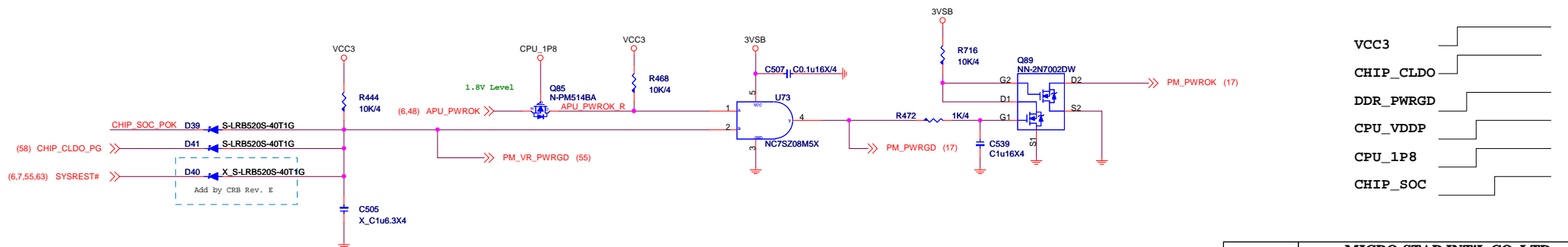
L04-68B7350-T15

CH-0.68u15A5ms-HF-1

1V@9A  
 OCP=16A



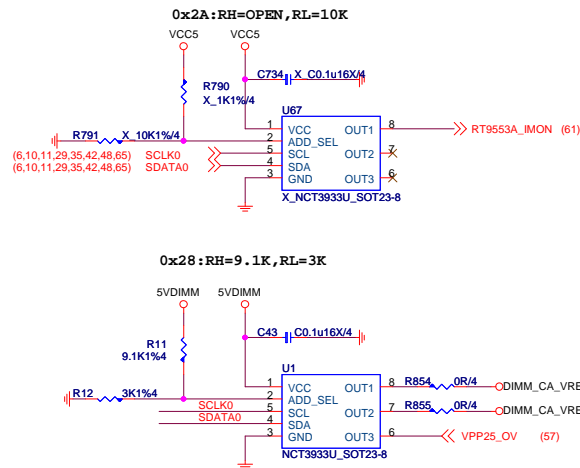
S0 PG



VCC3  
 CHIP\_CLDO  
 DDR\_PWRGD  
 CPU\_VDDP  
 CPU\_1P8  
 CHIP\_SOC

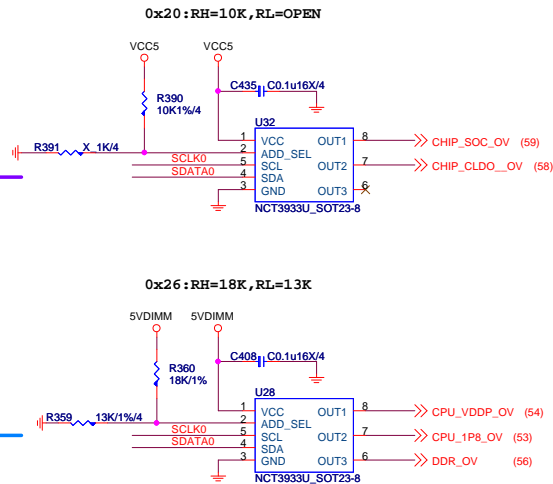
MICRO-STAR INT'L CO.,LTD			
MS-7C37			
Size	Document Description	Rev	
Custom	PROM - NB503 / 1.0V	2.1	
Date:	Friday, April 26, 2019	Sheet	59 of 75

# Over Voltage Control IC



## UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%



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## UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

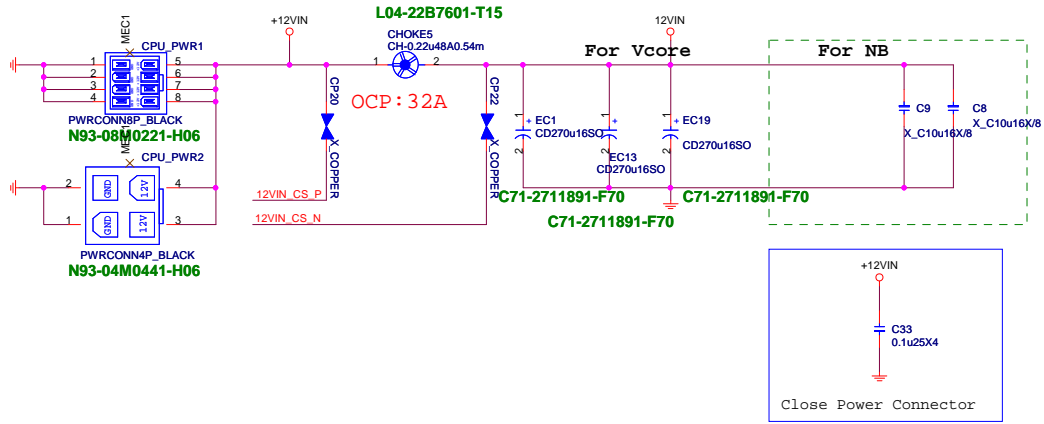


MICRO-STAR INT'L CO.,LTD

MS-7C37

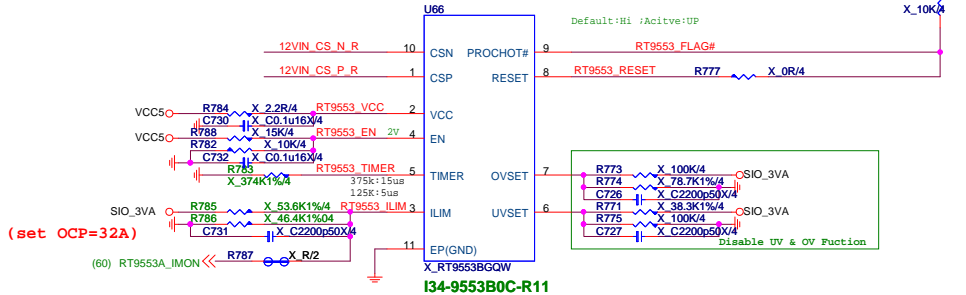
Size Custom	Document Description <b>OV Control - NCT3933</b>	Rev 2.1
Date: Friday, April 26, 2019	Sheet 60 of 75	

CPU POWER CONNECTOR



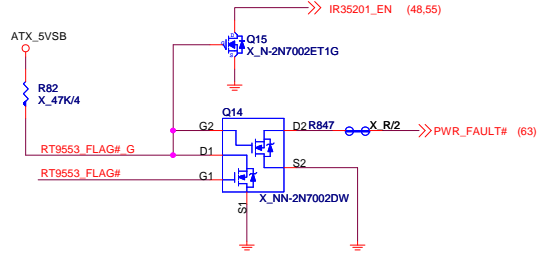
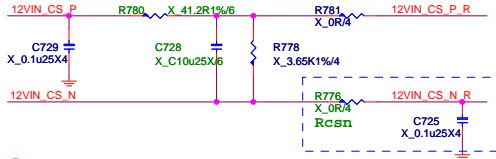
RT9553B CURRENT SENSE

RT9553 PIN5: When start OV/UV, RESET delay time can meet SPEC 15us.

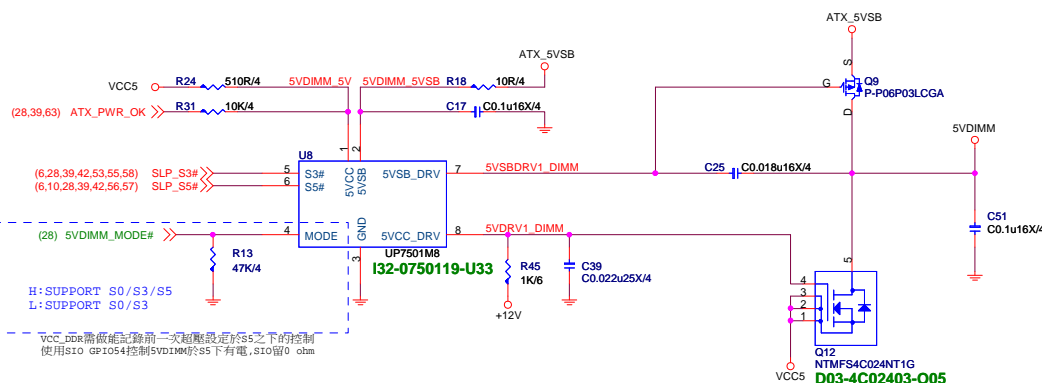


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Vcore		SOC	
D=Vout/Vin		D=Vout/Vin	
Vin = 12	> input voltage	Vin = 12	> input voltage
Vout = 2	> output Vcore	Vout = 1.55	> output Vcore
D = 0.166667		D = 0.129167	
Io = Icore(max)*0.8		Io = Icore(max)*0.8	
I core(max) = 200	> Vcore current	I core(max) = 75	> Vcore current
I avg. = 160	A	I avg. = 60	A
I ripple={ Io*√ D*√ (1-D) } / Phase		I ripple={ Io*√ D*√ (1-D) } / Phase	
Phase = 10	phase	Phase = 2	phase
I ripple = 5.962848	A	I ripple = 10.06153	A
How many pcs. Of Cap.		How many pcs. Of Cap.	
I ripple(cap) = 4700	m A	I ripple(cap) = 4700	m A
COETEMP = 1		COETEMP = 1	
Input Cap. = 2	pcs.	Input Cap. = 3	pcs.



## 5VDIMM FOR DDR



### 3VSB cost down

3.3V@3.363A

CPU: VDD\_33\_S5@0.25A

CHIP: VDD\_33\_S5@0.1A

PCIE\*4@1.5A

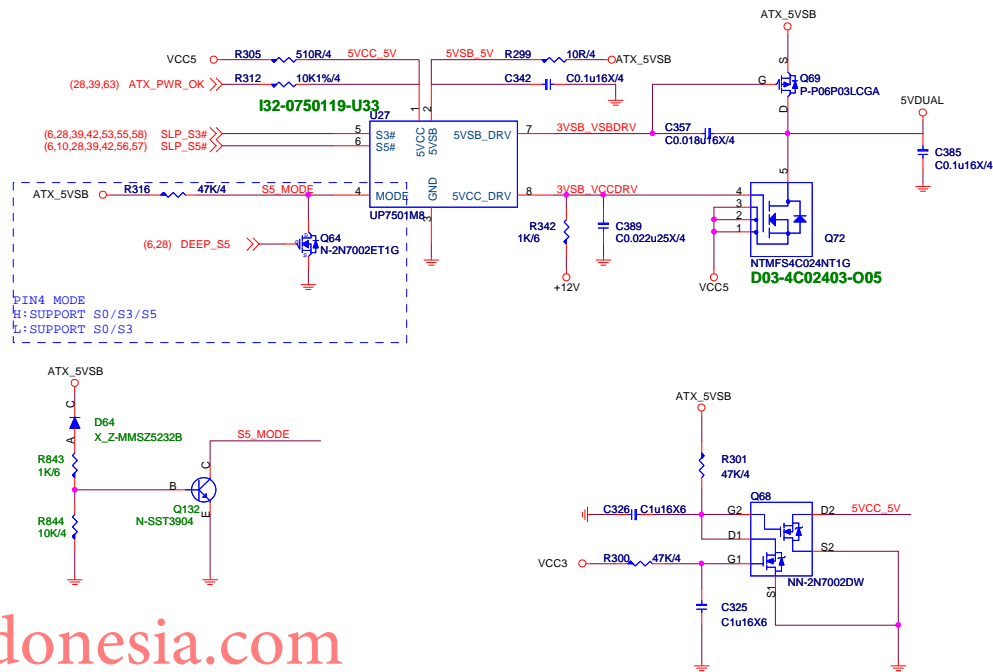
**M.2\_WIFI@0.78A**

LAN@0.065A

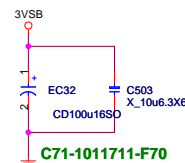
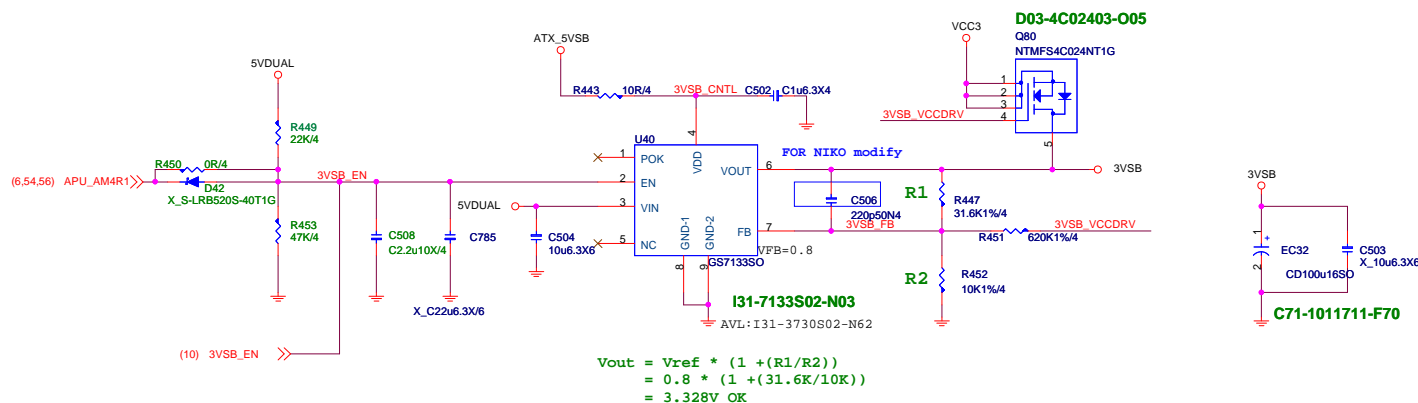
Redriver\*2@0.668A

USB TYPE-C@0.9mA

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```
| For power 700W solution (only for uP7501+uP7506 for 3VSB solution)|
| The power supply VCC3 delay 12ms after VCC5 assert.              |
| The chip U7501 5VDRV1 work when the VCC5 ready                  |
| (When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but    |
| VCC3 not ready and let the 3VSB sequence fail.                  |
```



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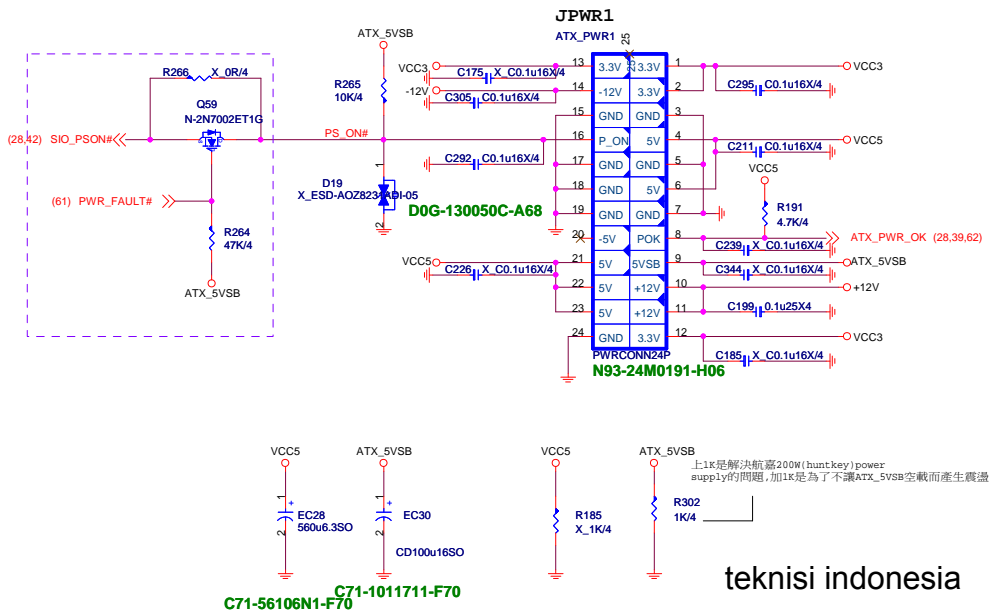
MS-7C37

Size Custom	Document Description <b>ACPI - 3VSB / 5VDIMM</b>	Rev 2.1
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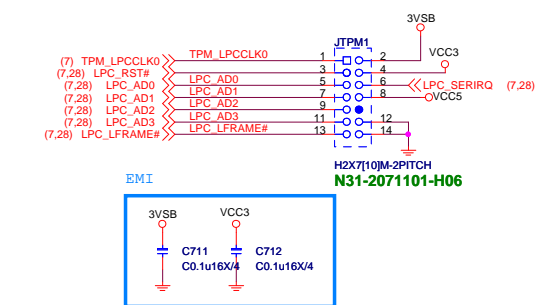
Date: Friday, April 26, 2019	Sheet 62 of 75
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## ATX POWER CONNECTOR



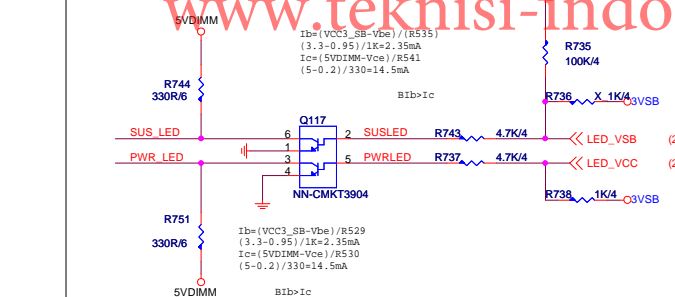
***TPM***



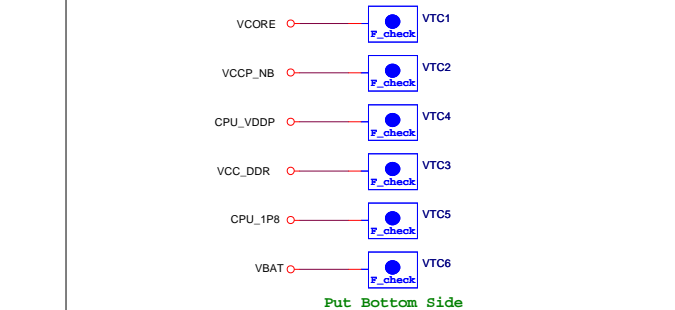
Add for EMI



## LED ( for NCT6797D)

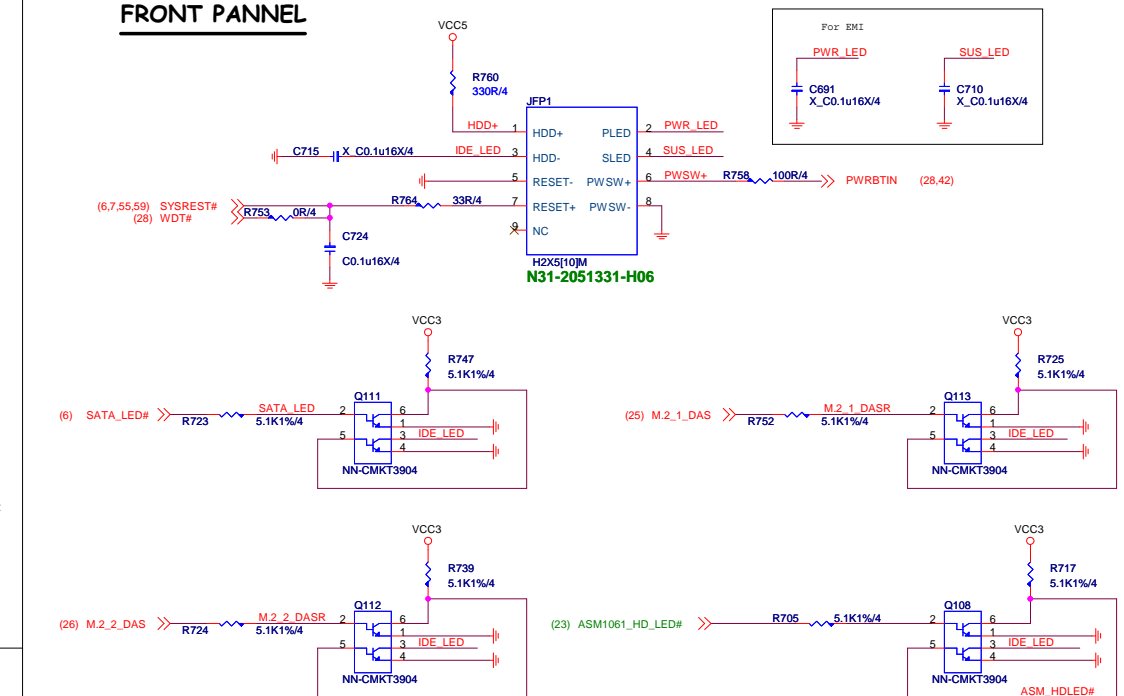


	Factory check point
--	---------------------

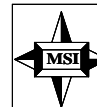
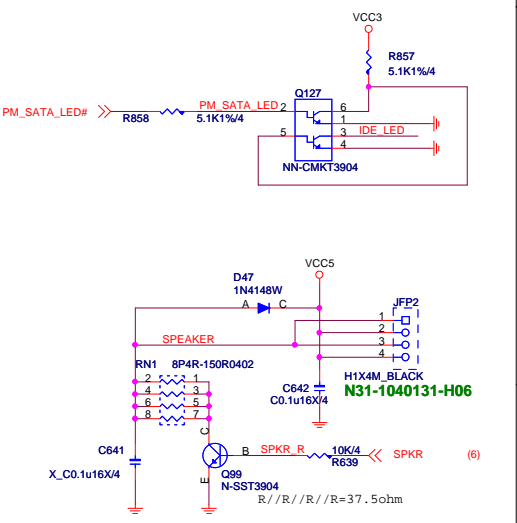
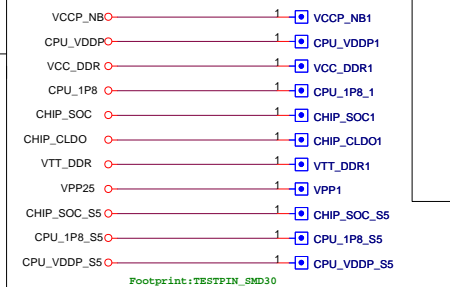


Put Bottom Side

FRONT PANNEL



**Voltage Mearsure Point**



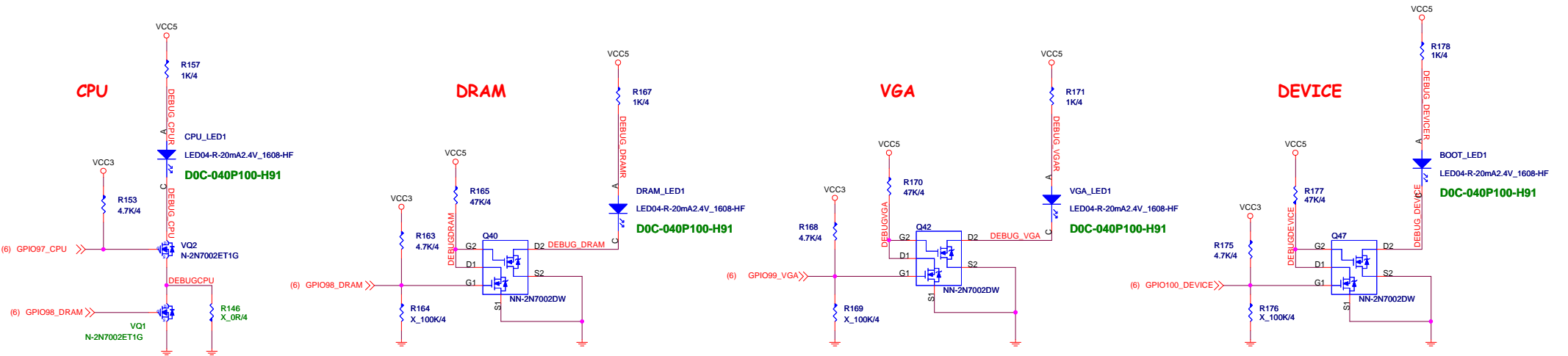
	<b>MICRO-STAR INT'L CO.,LTD</b>
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MS-7C37

Size Custom	Document Description <b>ATX Power - FrontPanel / EMI</b>	Rev 2.1
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EZ Debug LED



LED亮燈時同時將CPU LED關掉

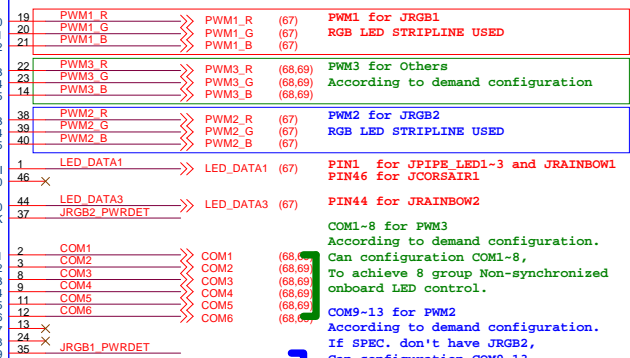
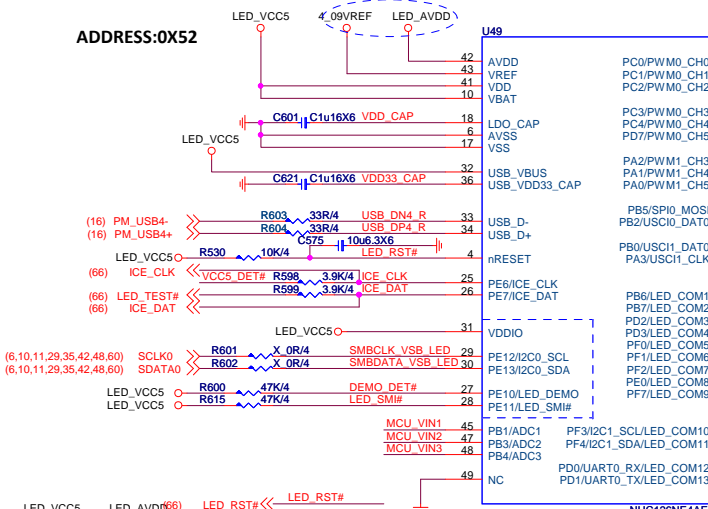
LEDGPIO	GPIO97	GPIO98	GPIO99	GPIO100
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

AMD AMP Detect LED

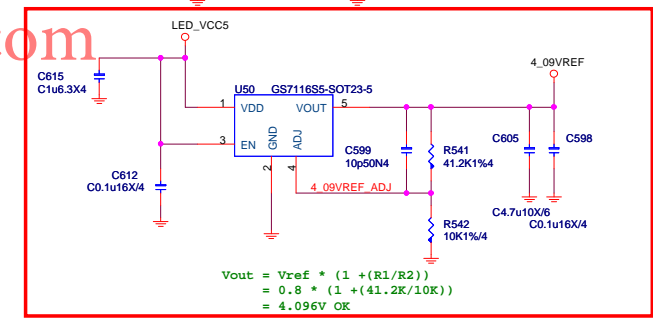
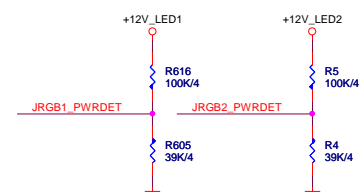
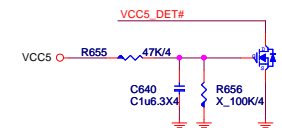
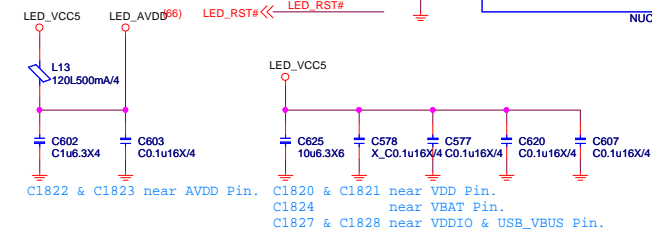
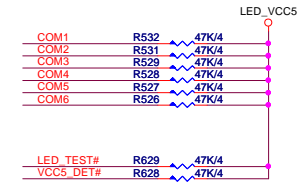
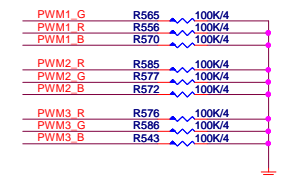
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## 48 PIN LED MCU

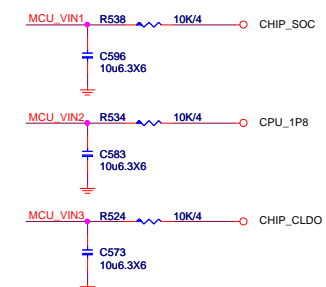
If you use ADC function, need to separate VREF from AVDD and 4\_09VREF stuff for VREF.



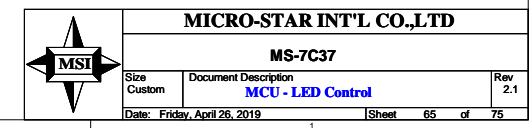
PS. COM1 is the first action block,  
next is COM2, and so on.  
Pin15,16 can configure to master  
smbus if spec requirement.



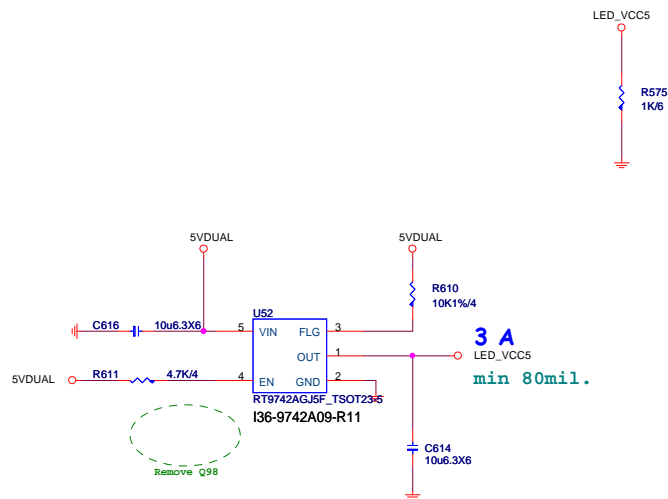
Option Spec For Voltage Monitor Require.



Control	Net Name	PWM USE
PCH	LED_DATA1	No Use
AUDIO Cover	LED_GPIO_01	No Use
MOS/IO cover	LED_GPIO_02	No Use
JRAINBOW1	LED_GPIO_03	No Use
JCORSAIR1	LED_DATA2	No Use
JRGB1/JRGB2	PWM1/ PWM2	PWM1/ PWM2
Board Side LED	COM 1-8	PWM3
Board Side LED	COM 9-13	PWM2

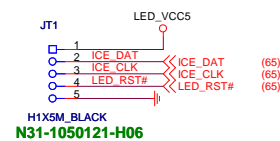


## EXTERNAL POWER INPUT



## External Power

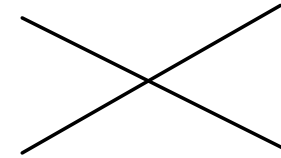
### JT1 for FW update



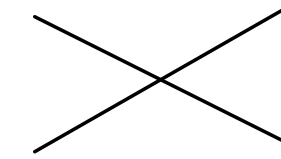
### JF1 For Factory Test



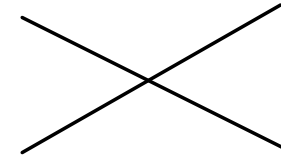
### 1 PCH HEATSINK LED



### 2 AUDIO/IO Cover LED



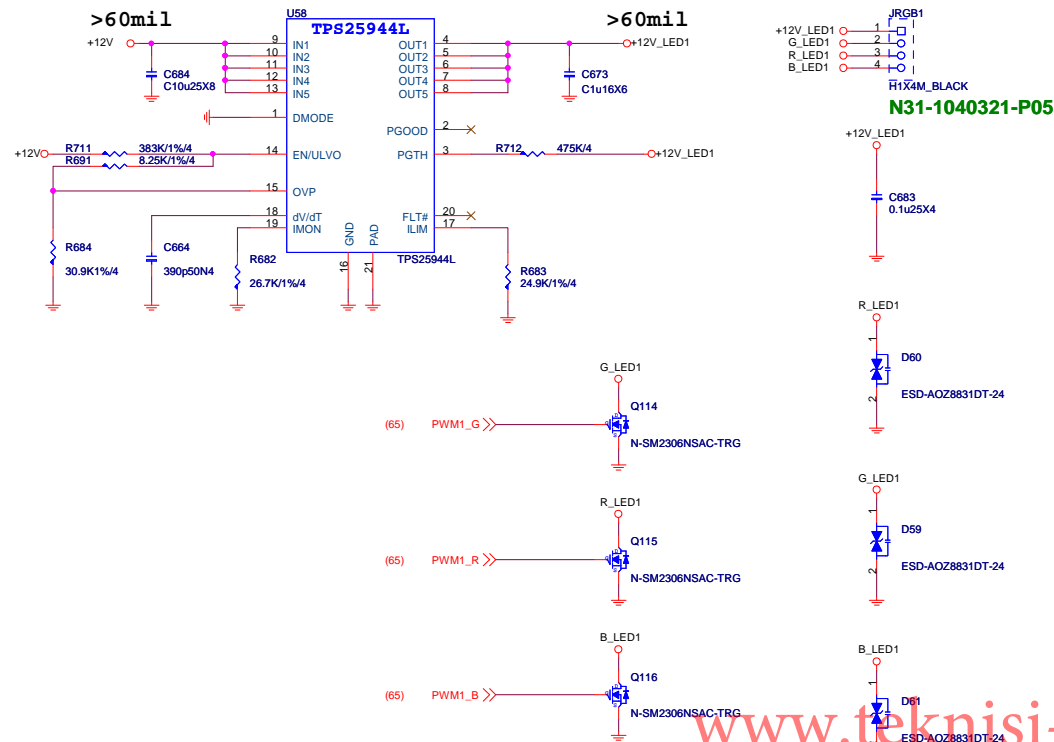
### 3 MOS HEATSINK LED



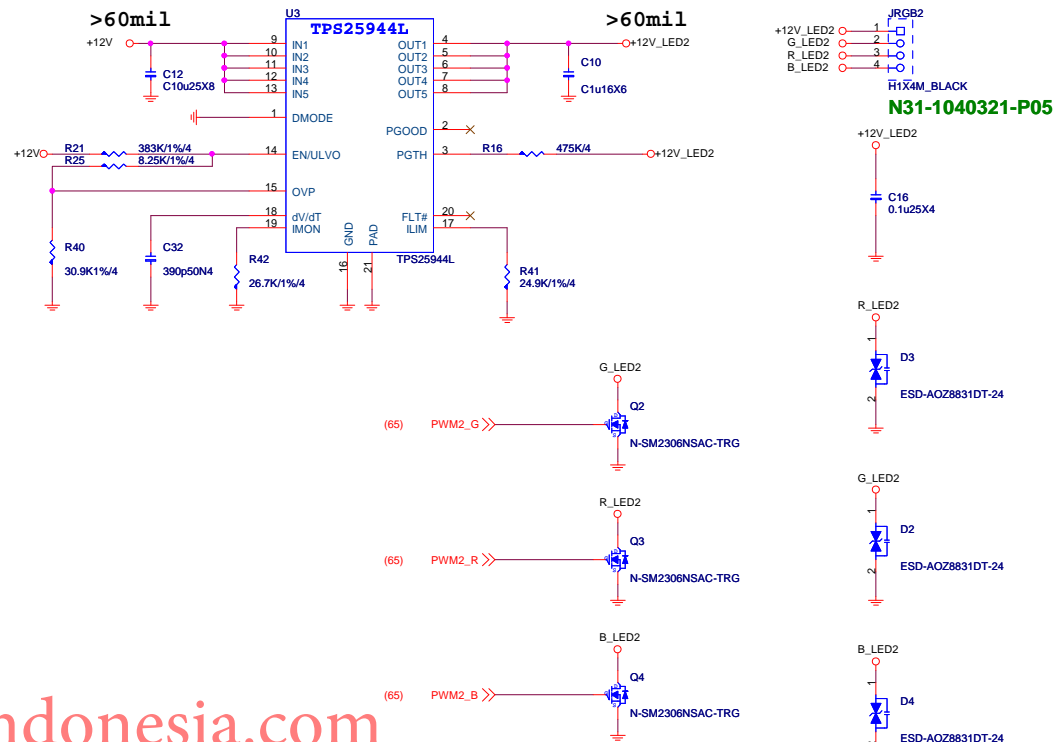
JPIPE:PIN1:output ,PIN2:input  
PIN2:MCU IN  
PIN1:HEATSINK OUT

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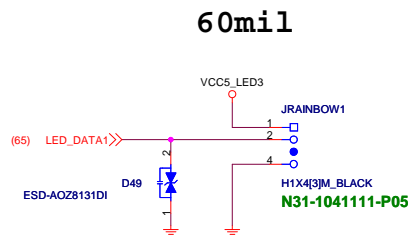
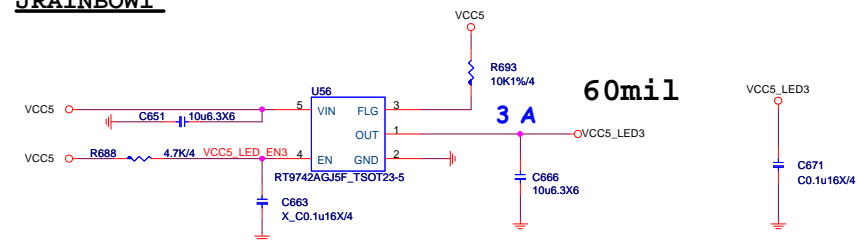
## JRGB1



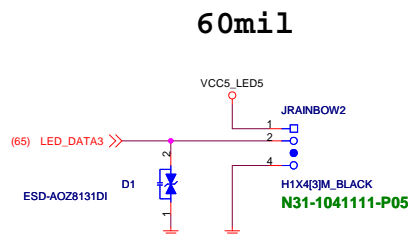
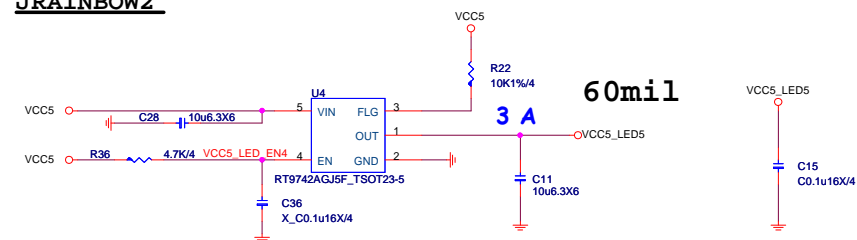
## JRGB2



## JRAINBOW1



## JRAINBOW2



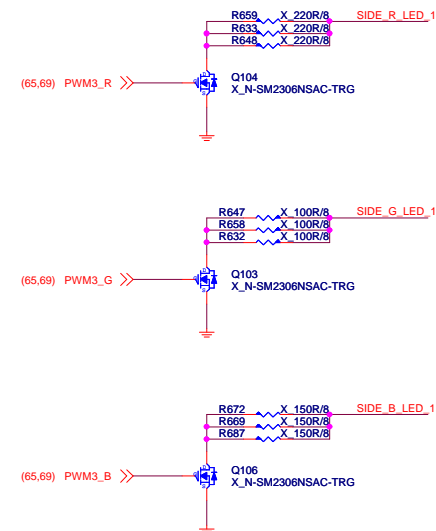
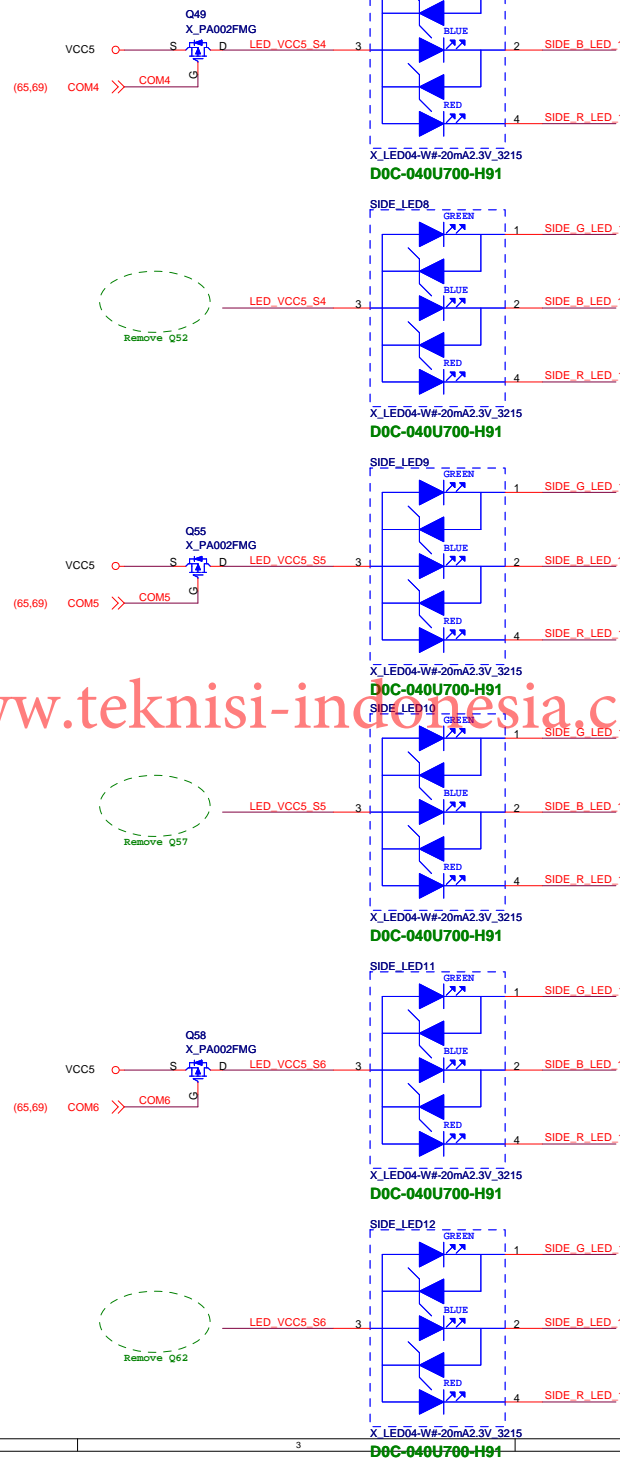
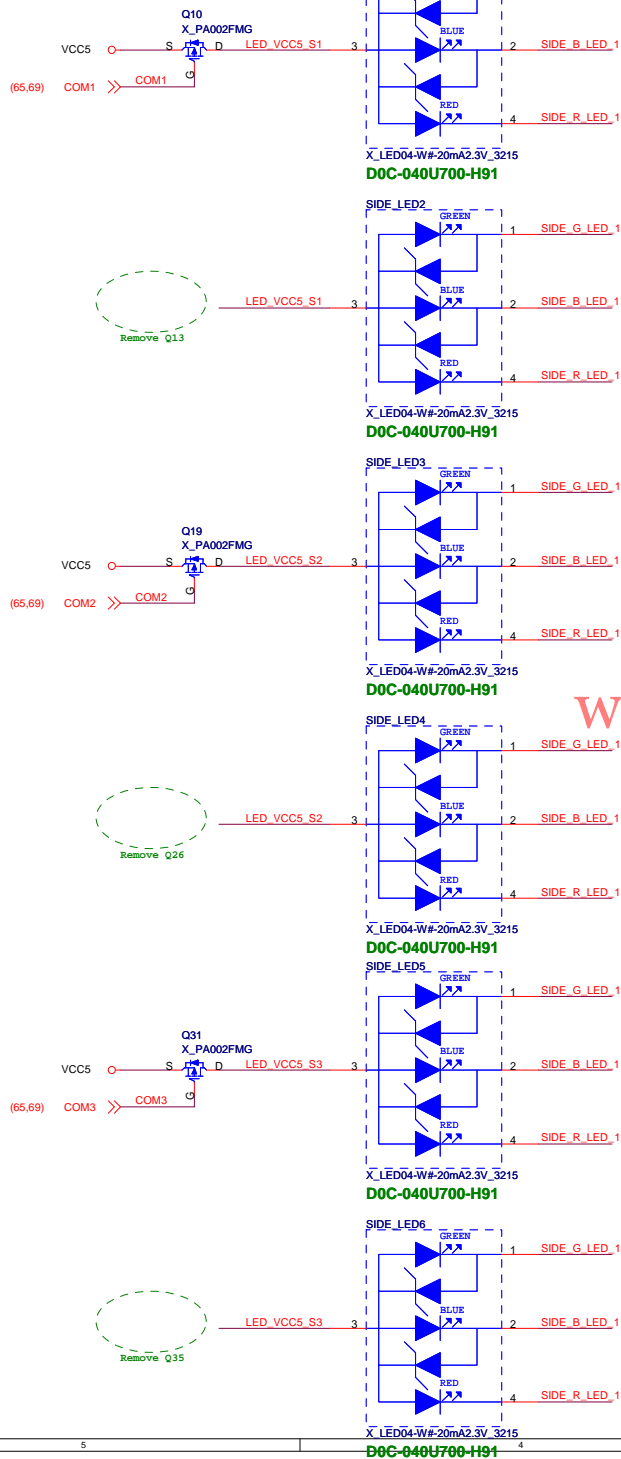
## JCORSAIR1

Vinafix.com



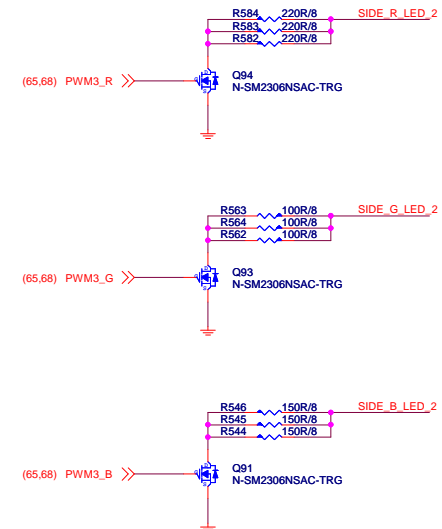
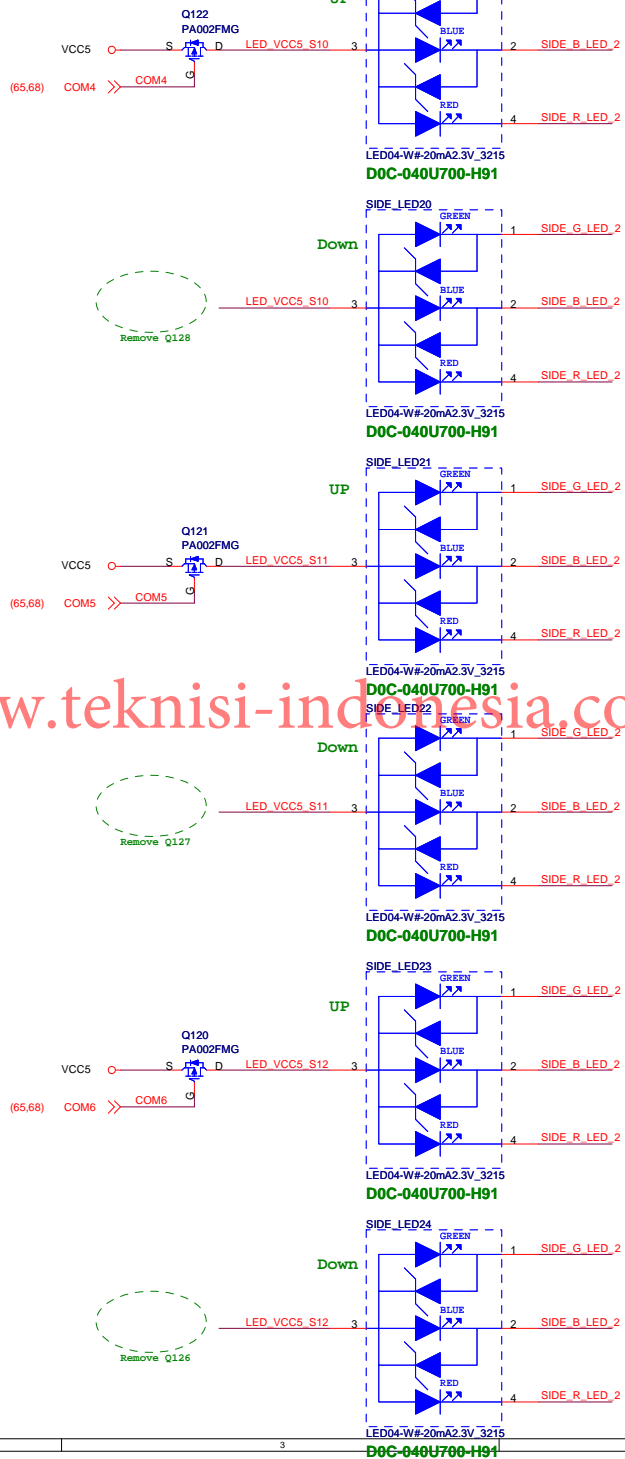
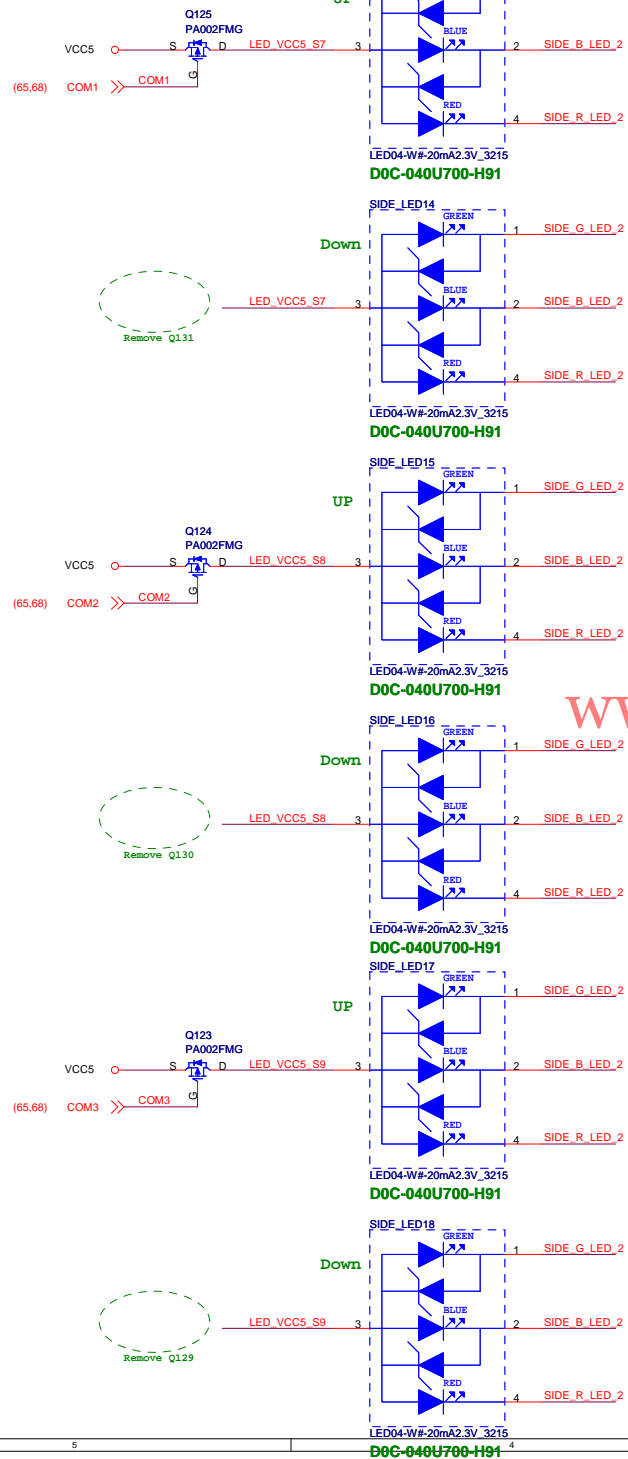
MICRO-STAR INT'L CO.,LTD		
MS-7C37		
Size Custom	Document Description	Rev 2.1
LED - JLED1 / 2 / 3 / 4		
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# Sidebar LED \*12



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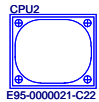
# Market Name LED \*12



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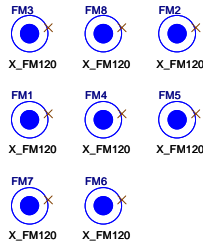
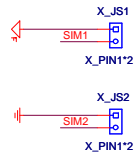
MSI		
MICRO-STAR INT'L CO.,LTD		
MS-7C37		
Size Custom	Document Description	Rev 2.1
LED - Market Name		
Date: Friday, April 26, 2019	Sheet 69	of 75

## CPU Socket

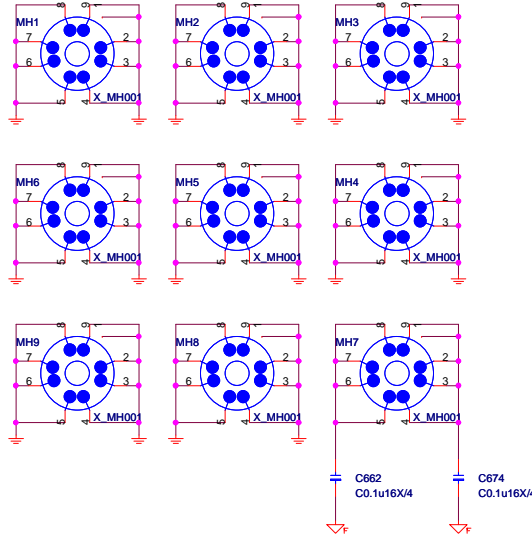


E95-0000022-C22

## Simulation



## Optics Orientation Holes



## MANUAL PART

UEFI1  
G51-M1SPXXA-A09  
G51-M1SPXXA-A09  
HDMI\_LA1  
Label  
HDMI  
HDMI LABEL  
Y01-RHDMI03-000

NAHIMIC1  
Y02-MU00100-NAH  
Y02-MU00100-NAH

XSPILT1  
X\_Y02-MA00401-XSP  
Y02-MA00401-XSP  
SSE1  
X\_Y02-MA00101-SSE  
Y02-MA00101-SSE



AVZ1  
D06-0100161-P52  
D06-0100101-X26

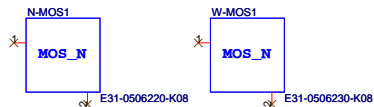
## PCB

PCB

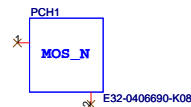


PD0-07C3721-E48

## MOS HEATSINK



## PCH HEATSINK



## Audio COVER



## IO COVER

## DDR COVER

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